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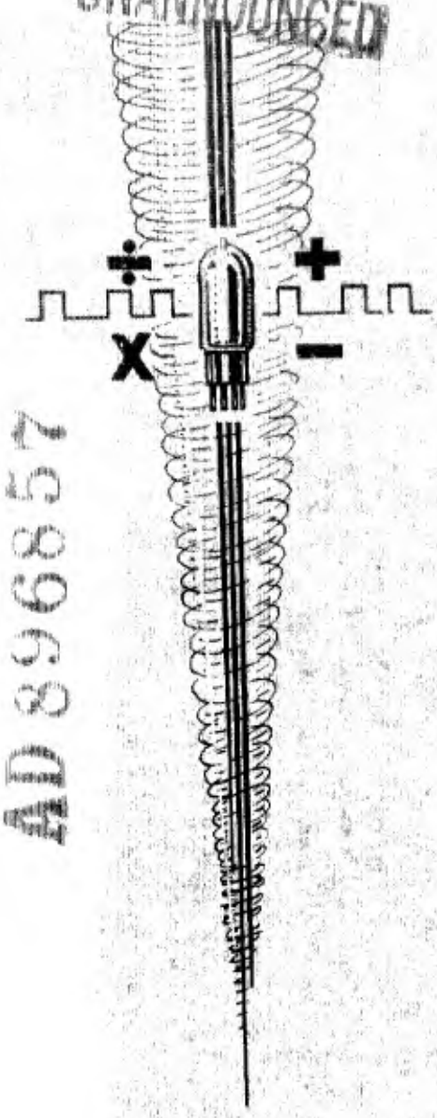

PROJECT
WHIRLWIND

Contract N5ori60

SUMMARY REPORT NO. 2

VOLUME 17

HIGH-SPEED SWITCHES

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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HIGH SPEED SWITCHES

Volume 17 of 22 Volumes

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Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

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INTRODUCTION

High-speed switches have many applications in the Whirlwind computers. With reference to the Block Diagrams of Vols. 5 and 6, and the System Drawings of Vol. 15, forms of such switches will be found in the time-pulse distributor, (Vol. 19, M-45), the operation-control (Vol. 5, p. 37) and the storage selection. Another application of switch techniques occurs in the connection between the accumulator flip-flops and the carry flip-flops (See Vol. 5, p. 26). The Project work on switches was started by David R. Brown as described in his thesis and further developed under his direction as reported in R-123 by John A. O'Brien, which report describes a 32-position switch with a set-up time of 0.2 microseconds.

R. C. Moses of Sylvania has constructed a satisfactory 8-channel time-pulse distributor based on this switch work but a report is not yet available.

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A HIGH-SPEED MULTI-POSITION ELECTRONIC SWITCH

by

DAVID R. BROWN
B. S., University of Washington
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Signature of Author..... /s/ David R. Brown
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Certified by..... /s/ Jay W. Forrester
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..... /s/ Harold L. Hazen
Chairman, Department Committee on Graduate Students

The writer is sincerely indebted to Mr. Jay W. Forrester for supervising this thesis and to all other members of the Project WHIRLWIND staff for their continued interest and assistance in the work. The writer is also grateful for the many facilities provided by the Servomechanisms Laboratory, under the direction of Professor Gordon S. Brown.

A HIGH-SPEED MULTI-POSITION ELECTRONIC SWITCH

ABSTRACT

Switches are discussed which, by means of an n-digit code, permit the selection of any one of 2^n load circuits. Since the thesis is concerned with multi-position switches for a high-speed digital computer, emphasis is on high-speed operation.

The type of switch believed to be the most promising is a high-speed multi-position switch employing a matrix of crystal rectifiers, the crystal matrix switch. An analysis of the switch and the establishment of a satisfactory design procedure are the objectives of the thesis.

A static analysis of the crystal matrix switch is presented which will permit the calculation of the voltages at the switch terminals for a general switch having 2^n terminals. A simple and useful equivalent circuit is derived.

The dynamic behavior, considering stray capacitances, is thoroughly discussed and an expression derived for the maximum switching time. The switching time is found to depend upon a single resistance in a leg of the matrix, R, and a shunt capacitance that can be estimated to a satisfactory degree of accuracy.

A design procedure is developed using the results of the analysis. Before the design is started, five factors must be known:

1. n, number of digits in the code
2. maximum switching time permissible
3. input resistance of the load circuit
4. input capacitance of the load circuit
5. change in voltage required to operate the load circuit

The following are determined by the design:

1. value of the resistor to be placed in the matrix
2. plate-supply voltage
3. type of tube required to drive the switch

An eight-position switch and a thirty-two position switch, for a switching time of 0.5 microsecond, are designed to illustrate the design procedure and show how the size and power requirements of the switch increase as the number of terminals increases.

The eight-position switch designed has been constructed and experiments are described which verify the analysis presented earlier. The measured switching time for the eight-position switch is 0.65 microsecond. Photographs of waveforms showing the operation of the switch are presented.

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INTRODUCTION

The thesis problem had its origin in Project WHIRLWIND, Servomechanisms Laboratory, Massachusetts Institute of Technology.

Project WHIRLWIND is engaged in the design and construction of a large-scale electronic digital computer. The computer will use the binary number system, the digit one being represented by a voltage pulse and the digit zero by the absence of a pulse. A parallel system will be used in which an n-digit binary number is transmitted simultaneously on n separate cables. The computer must operate at a very high speed; one number may follow another after as short a time as one microsecond. The voltage pulses will be nearly rectangular and one-quarter microsecond in duration.

Switches are needed which will permit the selection of one of a number of circuits. The thesis problem is to find the practical limitations of one type of switch that may be used, and to establish a satisfactory design procedure for that switch. The type to be considered is a high-speed multi-position electronic switch, using a matrix of crystal rectifiers. In the following pages, this type will be called the "crystal-matrix" switch.

The switches needed in the computer must operate in the following manner:

> The switch is to permit the selection of one of a number of circuits by means of a prearranged code. The code, or order, to set the switch will consist of

voltage pulses representing the digits of a binary number. All voltage pulses will arrive at the same time and at separate input terminals. Upon reception of the order, the switch must operate the circuit connected to the output terminal corresponding to the binary number in the order. If the order is an n-digit number, as many as 2^n output terminals may be incorporated in the switch. The voltage at the selected output terminal must be of sufficient amplitude to operate the circuit connected to that terminal and the voltage at any other terminal must not be of sufficient amplitude to operate the circuit connected to that terminal. The time required by the switch to operate the selected output circuit after reception of the order may be less than one microsecond. In addition, the switch must be capable of being reset to the zero position; the required reset time may be less than one microsecond.

Before the crystal-matrix switch is treated in greater detail, some various types of electronic switches will be discussed. This discussion will make possible a better understanding of the problem of high-speed multi-position switching.

HIGH-SPEED MULTI-POSITION ELECTRONIC SWITCHES

The simplest switch, the two-position switch, will be described first. Then, some various schemes of going from the two-position switch to a switch having more than two positions will be discussed. This presentation will show the logical development of the crystal-matrix switch and its advantages over other switching schemes.

Two-Position Switch

A resistance-coupled multivibrator, or flip-flop, may be used as a two-position switch. The circuit diagram of a flip-flop is shown in Drawing A-30520. The circuit has two stable states: first, V_1 conducting and V_2 non-conducting; second, V_1 non-conducting and V_2 conducting. The normal, or zero, state is V_1 conducting and V_2 non-conducting, indicated by shading V_1. When in the zero state, the plate of V_2 is at a higher voltage than the plate of V_1. If a negative pulse is applied to the set terminal, it will pass thru the crystal rectifier and cutoff V_1, causing the flip-flop to transfer to the other, or one, state. When in the one state, the plate of V_1 is at a higher voltage than the plate of V_2. The flip-flop may be returned to the zero state by the application of a negative pulse to the reset terminal.

A load circuit may be connected to each of the plate terminals of the flip-flop. The load circuit is biased so that when

the flip-flop is in the zero state, the load circuit connected to the plate of V_1, the 1 terminal, is inoperative and the load circuit connected to the plate of V_2, the 0 terminal, is operative. When the flip-flop is in the one state, the load circuit connected to terminal 1 is operative and the load circuit connected to terminal 0 is inoperative.

A convenient symbol for a flip-flop is also shown in Drawing A-30520. The symbol indicates a four-terminal circuit having set, reset, 1 and 0 terminals.

Flip-flops have been described extensively in the literature and considerable work has been done in Project WHIRLWIND to develop flip-flops suitable for use as two position switches.[1]

The load circuit most frequently used is a gate circuit. The circuit diagram of a gate circuit is shown in Drawing A-30521. Either the control grid or the suppressor grid can cutoff plate current. The control grid is normally biased below cutoff and the input will be a train of positive pulses. If the suppressor grid is connected to a non-selected terminal of the switch, the suppressor grid will be below cutoff and the input pulses will not appear at the output terminal. If the suppressor grid is connected to a selected terminal of the switch, the suppressor grid will be above cutoff and plate current will flow when the control grid is driven above cutoff, permitting the input pulses to appear at the output terminal.

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[1] O'Brien, John J., Investigation of Flip-Flop Circuits, Project WHIRLWIND Report No. R-113, March 19, 1947.

A symbol for a gate circuit is also shown in Drawing A-30521. The symbol indicates a three-terminal circuit having input and output terminals and a terminal which can be connected to the switch.

The characteristics of various types of gate circuits have been investigated in Project WHIRLWIND.[1]

A two-position switch which controls two output channels is shown in Drawing A-30522. Here the switch is used to select the output terminal at which the input pulses are to appear. The switch order is applied to the set terminal of the flip-flop. If the order is a zero, as indicated by the absence of a pulse, the input pulses will appear at output terminal 0. If the order is a one, as indicated by the presence of a pulse, the flip-flop will switch and the input pulses will appear at output terminal 1. A pulse applied to the reset terminal of the flip-flop will reset the switch to the zero position.

Gate-Tube Whiffle-Tree Switch

Two-channel switches of the type shown in Drawing A-30522 may be cascaded to form a multi-channel switch. Cascading the gate tubes gives the appearence of a whiffle tree as shown in Drawing A-30523. An eight-position whiffle-tree gate-tube switch is shown.

The switch operates as follows:

The order and output terminals have been assigned binary numbers. A three-digit order is applied to the three order terminals. The output termina

[1] Brown, David R., Gate Circuits, Project WHIRLWIND, Report No. R-109, December 17, 1946.

corresponding to the binary number of the order will be selected. For example, suppose the binary number of the order is 101. Voltage pulses are applied to order terminals 1 and 100, switching the corresponding flip-flops. An inspection of Drawing A-30523 shows that the input pulses will appear at output terminal 101. A pulse applied to the reset terminal will reset the switch to the zero position.

Although an eight-position switch is shown in Drawing A-30523, a generalization to the 2^n-position switch can easily be made.

The switch requires a large number of gate tubes, $2^{n+1}-2$ for a 2^n-position switch. A more important disadvantage, however, is that the input pulses must go through n gate tubes in series, which will lengthen and delay the pulses.

Multi-Grid Gate-Tube Switch

The whiffle-tree gate-tube switch uses gate tubes which have one control grid to which input pulses may be applied and one grid for switching. If a gate tube having n switching grids instead of one is available, the disadvantages of the whiffle-tree switch may be overcome. The diagram of a multi-grid gate-tube switch for an n of 3 is shown in Drawing A-30524. The operation is the same as for the whiffle-tree switch. The multi-grid gate-tube switch has been studied by Rubinoff.[1]

The disadvantage of the multi-grid gate-tube switch is the difficulty of obtaining a gate tube having more than one switching grid.

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[1] Rubinoff, Morris, An Input Device Using Multiple Gates, a paper presented at A Symposium of Large Scale Digital Calculating Machinery, Harvard University, January 10, 1947.

Resistance-Matrix Switch

A modification of the multi-grid gate-tube switch which eliminates the necessity of multi-grid gate tubes has been suggested and analyzed by Crawford.[1] This modification introduces a matrix of resistors as shown in Drawing A-30525. Also, to drive the resistance matrix and isolate it from the flip-flops, buffer amplifiers, symbol BA, are used.

Crawford's analysis of the resistance-matrix switch is summarized in the following two paragraphs:

> Suppose that the plate voltage of an "off" buffer amplifier is 100 volts and the plate voltage of an "on" buffer amplifier is zero. If the binary number of the switch order is 101, matrix terminal 101 will be 100 volts. Matrix terminals 1, 100, and 111, will be at 66-2/3 volts. Matrix terminals 0, 11, and 110, will be at 33-1/3 volts. The voltage of matrix terminal 10 will be zero. This assumes that the source resistance of the buffer amplifiers is very low compared to the resistance of the matrix as seen by the buffer amplifiers. Also, the circuit connected to the matrix terminal is assumed to have very high input resistance. If the switch is to select only one of the circuits connected to the matrix terminals, the voltage necessary to operate the circuit must be greater than 66-2/3 volts and less than 100 volts.
>
> The distribution of voltages of the matrix terminals is given by the coefficients in the binomial expansion $(1 \oplus 1)^n$.[2] if n is two, and the same conditions are assumed, the voltage of one terminal will be 100 volts, two will be at 50 volts, and the voltage of one terminal will be zero. If n is four, one terminal will be at 100 volts, four will be at 75 volts, six will be at 50 volts, four will be at 25 volts, and the voltage of one will be zero.

Notice that although only one switching grid is required in the gate tubes, only a fraction of the voltage change at the buffer

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[1] Crawford, Perry O., Automatic Control by Arithmetic Operations, Master's Thesis, Physics Dept., Mass. Inst. of Tech. 1942.

[2] $(1 \oplus 1)^n = 1 \oplus n \oplus \frac{n(n-1)}{2!} \oplus \frac{n(n-1)(n-2)}{3!} \oplus \ldots$

amplifier appears at the matrix terminals as a useful switching voltage. If the change in voltage at the buffer amplifier is $\triangle E'$, the useful switching voltage is $\triangle E'/n$. The useful switching voltage is defined as the minimum voltage difference between the selected terminal and any non-selected terminal.

Crystal Matrix Switch

A further modification has been suggested which will permit a larger useful switching voltage.[1] The resistors of the resistance matrix are replaced by crystal rectifiers as shown in Drawing A-30526. The advantage of the crystal matrix switch over the resistance matrix switch is that nearly the full change in voltage at the plate of a buffer amplifier is available at the terminals of the crystal matrix. The number of crystal rectifiers required is $n2^n$.

The function of the crystal matrix can be seen more readily if the matrix is redrawn as in Drawing A-30527. Plate current for the buffer amplifiers must flow thru the resistors, R. The crystal matrix is connected so that current always flows through all but one of the resistors. The terminal associated with that resistor, being at a higher voltage than the other terminals, is the selected terminal.

An analysis of the 2^n-position switch of the type shown in Drawing A-30527, and the establishment of a satisfactory design procedure, are the objectives of this thesis.

---

1 The writer became acquainted with this suggestion at a course on electronic digital computers given at the Moore School of Electrical Engineering, University of Pennsylvania, during the summer of 1946.

Since the analysis and design of flip-flops and gate circuits are well established, attention will be focused on the buffer amplifiers and the crystal matrix.

ANALYSIS OF THE CRYSTAL-MATRIX SWITCH

Both the static and the dynamic behavior will be analyzed; the static analysis will be presented first. The method of first considering a switch with a small number of terminals, then a larger number, and progressing gradually to the general case will be followed.

Static Analysis

The static analysis will be made only for the case where the zero terminal is the selected terminal. The distribution of voltages at the matrix terminals for any other terminal as the selected terminal may be inferred from the analysis to be presented.

The circuit diagram of a four-position crystal-matrix switch is shown in Drawing A-30528. The analysis is complicated by the fact that the crystal rectifiers are non-linear elements. The voltage-current characteristic of a typical 1N34 germanium-crystal rectifier is shown in Drawing A-38201-G. In order to make a simple analysis possible, the crystal-rectifier will be assumed to have a forward resistance, R_f, and a back resistance R_b, which are independent of the magnitude of the current through the rectifier. To determine whether a crystal rectifier may be

represented by R_f or R_b, the polarity of the voltage across the rectifier must be established. This can be done by an inspection of the circuit. An "on" buffer amplifier may be represented by the static plate resistance of the tube, R_p; an "off" buffer amplifier, by an infinite resistance. If these equivalent resistances are used, the circuit diagram of Drawing A-30528 becomes the equivalent circuit of Drawing A-30529. If R_f is assumed to be much smaller than R, the equivalent circuit becomes the simplified equivalent circuit of Drawing A-30529. Since R_f is the order of 100 ohms, this is a reasonable assumption for an R greater than 1,000 ohms.

The circuit diagram of an eight-position crystal-matrix switch is shown in Drawing A-30530. An equivalent circuit of the eight-position switch is shown in Drawing A-30531. If R_f is assumed to be much smaller than R, the equivalent circuit becomes the simplified equivalent circuit of Drawing A-30531.

The circuit diagram of a sixteen-position switch is shown in Drawing A-30532. The equivalent circuit and simplified equivalent circuit are shown in Drawing A-30533.

Note that the validity of the assumption that R_f may be neglected if R_f is much smaller than R is not affected as the number of terminals increases.

An inspection of the simplified equivalent circuits of the four, eight, and sixteen-position switches will permit the equivalent circuit of the general case to be established. The simplified equivalent circuit of the 2^n-position switch is shown

in Drawing A-30534. The useful switching voltage, ΔE, is the voltage difference between the selected and the non-selected terminals. The simplified equivalent circuit shows that ΔE will decrease as n increases or R_b decreases. Although R_b may be much greater than R, it cannot be neglected; it appears in the equivalent circuit divided by $n(2^{n-1}-1)$. The useful switching voltage, ΔE, may be calculated from the equivalent circuit.

Let,

$$\frac{R}{2^n - 1} = R_1$$

and,

$$\frac{R_b}{n(2^{n-1}-1)} = R_2$$

The circuit for calculation of ΔE, shown in Drawing A-30534, may be obtained directly from the simplified equivalent circuit by use of Thevenin's Theorem. Then,

$$\Delta E = \left(\frac{nR_1}{nR_1 + R_p}\right) \left(\frac{R_2}{\frac{R_1 R_p}{nR_1 + R_p} + R + R_2}\right) E_{bb}$$

$$= \left(\frac{nR_1 R_2}{R_1 R_p + nR_1 R + R_p R + nR_1 R_2 + R_2 R_p}\right) E_{bb}$$

$$= \frac{nR_1 R_2 E_{bb}}{R_p(R + R_1 + R_2) + nR_1(R + R_2)}$$

where,

R = resistance from the plate supply to a horizontal wire of the matrix

R_f = forward resistance of a crystal rectifier

R_b = back resistance of a crystal rectifier

n = number of flip-flops

E_{bb} = plate-supply voltage

$$R_1 = \frac{R}{2^{n-1}}$$

$$R_2 = \frac{R_b}{n(2^{n-1}-1)}$$

and

$$R_f \ll$$

Dynamic Analysis

The objective of the dynamic analysis is a quantitative expression for the switching time. The four-position switch of Drawing A-30535 will be considered first. Before any attempt is made to represent the switching transients quantitatively, the operation of the switch must be thoroughly understood. Such an understanding will permit a great simplification of an otherwise complicated problem.

When studying operation at terminal 0 as typical, six transitions are of interest in the four-position switch:

a. from terminal 0 to terminal 1
b. from terminal 1 to terminal 0
c. from terminal 0 to terminal 2
d. from terminal 2 to terminal 0
e. from terminal 0 to terminal 3
f. from terminal 3 to terminal 0

For transition (a) to take place, the 1 flip-flop must switch, cutting off V_1 and driving on V_2. Since the wavefronts from the flip-flop have finite rise time, and V_2 is initially biased well below cutoff, V_1 will cutoff before V_2 will be driven on. Let V_1 and V_2 be represented by an R_p in series with a switch as shown in Drawing A-30536. Switch S_1 opens at time t_1 and switch S_2 closes at time t_2. Since the polarity of the voltage across some of the crystals will change during the switching process, a crystal rectifier cannot be represented by a resistance. For the dynamic analysis, assume that R_f is zero and R_b is infinite and let the crystal be represented by a switch. The assumption of zero R_f has been justified previously. The assumption of an infinite R_b will lead to a more conservative expression for the switching time, as will be seen later, and will help to simplify the problem. The switch is open if the voltage is in the back direction and closed if the voltage is in the forward direction. If the polarity across the crystal does not change, the crystal may be represented by a short circuit or an open circuit. For example, Crystal A of Drawing A-30535 will have a forward voltage across it during the entire switching period and may be represented by a short circuit as shown in Drawing A-30536. Crystal B

initially has a forward voltage across it but the voltage across the crystal reverses in polarity as soon as V_2 begins to conduct and draw plate current through the R associated with terminal 0. Crystal B is therefore represented as a switch which opens at time t_2.

The waveforms at the four terminals of the switch are shown in Drawing A-30536 and the equivalent circuits for any particular time interval are shown in Drawing A-30537. Initially, terminal 0 is the selected terminal and terminals 1, 2, and 3, are at some lower voltage. At time t_1, S_1 opens and the voltage at terminal 1 increases. Shunt capacitance will prevent the voltage from changing instantaneously. Also at time t_1, the voltage at terminals 2 and 3 will increase. This may be explained as follows. Initially, terminals 2 and 3 are at the normal non-selected voltage, $E_{(n-s)}$.

$$E_{(n-s)} = \frac{\frac{R_p}{2}}{\frac{R_p}{2} + \frac{R}{3}}$$

$$= \frac{R_p}{R_p + \frac{2R}{3}}$$

During the switching transition, until some time after t_2, terminals 2 and 3 will charge toward a temporary final value, $E_{(tfv)}$, greater than $E_{(n-s)}$. As may be seen from the equivalent circuit.

$$E_{(tfv)} = \frac{R_p}{R_p + \frac{R}{2}}$$

since

$$\frac{R_p}{R_p + \frac{R}{2}} > \frac{R_p}{R_p + \frac{2R}{3}}$$

$$E_{(tfv)} > E_{(n-s)}$$

The voltage at terminals 2 and 3 may tend to increase more rapidly than the voltage at terminal 1. In this case, S_G will remain closed until time t_x when the voltage across Crystal G reverses. Until time t_x, terminals 1, 2, and 3, will rise together.

At time t_2, S_2 closes and S_B opens, lowering the voltage at terminal 0. At time t_3 the voltage at terminal 0 reaches the voltage at terminals 2 and 3; S_E closes and the voltage at terminals 0, 2, and 3, returns to the normal non-selected voltage. Note that a transient would be observed at terminals 2 and 3 even if S_1 and S_2 were switched simultaneously. Terminal 1, after time t_x, increases in voltage as the shunt capacitance is charged through the resistor, R. At the end of the transient when terminal 1 reaches its final value, at time t_5, S_D closes. The switching time $t_4 - t_1$, is determined almost entirely by the length of time required to charge the shunt capacitance through the resistor R. During most of the switching transient, the shunt capacitance is that associated with one horizontal wire and one

vertical wire of the matrix. In general, the terminal being selected will be the last terminal to arrive at its final voltage.

The dashed lines on the waveforms indicate the effects of capacitance coupling between parts of the switch and will be discussed later.

As yet only transition a, from terminal 0 to terminal 1 has been discussed. The waveforms for transition b will be the same as those shown in Drawing A-30536 except that the waveforms at terminals 0 and 1 will be interchanged. Transition c will be the same except that the waveforms at terminals 1 and 2 will be interchanged. The waveforms for transition d will be the same as those for transition c with the waveforms at terminals 0 and 2 interchanged.

Transition e from terminal 0 to terminal 3, will be different because both flip-flops will be switched. The equivalent circuit and the waveforms at the output terminals are shown in Drawing A-30538. The equivalent circuit for any particular time interval may be found in Drawing A-30539. At time t_1, S_1 and S_3 open and the voltage of terminals 1, 2, and 3, increases. At time t_2, S_2 and S_4 close decreasing the voltage at terminal 0. At time t_3, the voltage at terminal 0 reaches the voltage at terminals 1, 2, and 3; S_C and S_F open and S_D and S_E close. After time t_3, the voltage of terminals 0, 1, and 2, returns to the normal non-selected voltage and the voltage of terminal 3 continues to

increase. The voltage of terminal 3 increases as the shunt capacitance C, is charged through the resistor R. Again, the switching time is largely determined by the time constant, RC. The capacitance, C, is that associated with one horizontal wire of the matrix and two vertical wires, a larger shunt capacitance than that charged in the transition from terminal 0 to terminal 1. In general, the transition which will require the longest switching time occurs when all n flip-flops are switched.

The waveforms for transition f, from terminal 3 to terminal 0, will be the same as those for transition e with the waveforms at terminals 0 and 3 interchanged.

A similar analysis can be made of the eight-position switch. The fourteen possible transitions involving the terminal 0 are:

a. from terminal 0 to terminal 1
b. from terminal 1 to terminal 0
c. from terminal 0 to terminal 2
d. from terminal 2 to terminal 0
e. from terminal 0 to terminal 3
f. from terminal 3 to terminal 0
g. from terminal 0 to terminal 4
h. from terminal 4 to terminal 0
i. from terminal 0 to terminal 5
j. from terminal 5 to terminal 0
k. from terminal 0 to terminal 6
l. from terminal 6 to terminal 0
m. from terminal 0 to terminal 7
n. from terminal 7 to terminal 0

These fourteen transitions reduce to three basic types; just as the seven possible transitions for the four-position switch reduced the two basic types. The three types of transitions for the eight-position switch are:

1. One flip-flop switched.

2. Two flip-flops switched.

3. Three flip-flops switched.

Transitions a, b, c, d, g, and h, are the first type. Transitions e, f, i, j, k, and l, are the second type. Transitions m and n are the third type.

A circuit diagram of the eight-position switch appears in Drawing A-30540. The equivalent circuits and the waveforms for the three basic types, transitions a, e, and m, are shown in Drawings A-30541, A-30542, A-30543, A-30544, A-30545, and A-30546.

The preceding analysis has neglected capacitance coupling between the various parts of the switch. The capacitance between adjacent parts has been assumed to be small compared to the capacitance to ground of any part. The effect of capacitance coupling would be in the direction indicated by the dashed curves on the waveforms.

The analysis, although qualitative, yields some useful results.

1. The longest transition occurs when all n flip-flops are switched.

2. The terminal requiring the longest switching time is the terminal being selected.

3. The long portion of the transient at the terminal being selected is a simple R-C transient having a time constant equal to the product of R and the shunt capacitance C. It is not a function of R_p.

4. Transients will be observed at non-selected terminals. The amplitude of the transients

will depend upon which transition is being effected and on the delay, $t_2 - t_1$.

5. The transient at a non-selected terminal will subside at the same time that the terminal previously selected returns to the non-selected voltage.

The switching time τ, is defined as the time required for the voltage at the terminal to reach ten per cent of $\triangle E$ of its final value. The longest switching time τ_m will be at the terminal selected when all n flip-flops are switched. Since the longest switching time is the only important one, only the longest switching time will be treated quantitatively. To be useful, the expression for τ_m must be simple.

As shown previously, the time constant of the longer portion of the transient at the terminal being selected is RC, where C is the shunt capacitance. If the entire transient is assumed to have a time constant, RC, a conservative figure for the switching time may be obtained very easily. The voltage change is $\triangle E$. The problem is to find C.

A circuit diagram of the four-position switch showing the shunt capacitances is shown in Drawing A-30547. The parts of the matrix which increase in voltage an amount $\triangle E$ when both flip-flops are switched are indicated by heavy lines. In order to estimate the total shunt capacitance, C, assume that the parts indicated are the only ones that change in voltage and consider all the other parts to be at ground potential. The capacitances indicated are then defined as follows:

C_1 Interelectrode capacitance of a crystal rectifier.

C_2 Capacitance to ground of a crystal rectifier.

C_3 Output capacitance of buffer amplifier plus the capacitance to ground of a vertical wire of the matrix.

C_4 Input capacitance of the load circuit plus the capacitance to ground of a horizontal wire of the matrix.

For the four-position switch,

$$C = 2C_1 + 2C_2 + 2C_3 + C_4$$

The circuit diagram of the eight-position switch showing the shunt capacitances is shown in Drawing A-30548.

$$C = 9C_1 + 3C_2 + 3C_3 + C_4$$

The expression for C may now be generalized to the 2^n - position switch.

$$C = n(2^{n-1}-1)\, C_1 + n(C_2 + C_3) + C_4$$

The maximum switching time will be equal to 2.3 time constants.

$$\tau_\Delta = 2.3\ RC$$

DESIGN PROCEDURE

In the previous section, general expressions were obtained for the useful switching voltage, $\triangle E$, and the maximum switching time, τ_m. In this section, the results of the previous section will be used to establish a general design procedure. Several switches will be designed to illustrate the design procedure and the limitations of the switch.

General Design Procedure

The following factors must be known before the design is started:

1. n, number of flip-flops
2. τ_m, maximum switching time permissible
3. R_l, input resistance of the load circuit
4. C_l, input capacitance of the load circuit
5. $\triangle E$, useful switching voltage required

The following are to be determined by the design:

1. R_L, value of the resistor to be placed in the matrix
2. E_{bb}, plate-supply voltage
3. Tube Type for buffer amplifier

The first step in the design is to choose an E_{bb} and a tube type; this determines the output capacitance of the buffer

amplifier. The number of flip-flops, n, is known. Make a sketch of the physical arrangement of the matrix. Estimate the capacitance to ground of a vertical wire of the matrix and add it to the output capacitance of the buffer amplifier to obtain C_3. Estimate the capacitance to ground of a horizontal wire of the matrix and add it to the input capacitance of the load circuit to obtain C_4. Also, estimate the capacitance to ground of a crystal rectifier, C_2. The interelectrode capacitance of a crystal rectifier, C_1, is known or may be measured.

Now C may be calculated.

$$C = n(2^{n-1}-1)\, C_1 + n(C_2 + C_3) + C_4$$

The dynamic analysis has shown that

$$\tau_m = 2.3RC$$

Calculate R.

$$R = \frac{\tau_m}{2.3C}$$

Now, R is simply R_1 and R_L in parallel. Then,

$$R_L = \frac{RR_1}{R_1 - R}$$

The static analysis has shown that

$$E = \frac{nR_1 R_2 E_{bb}}{R_p (R + R_1 + R_2) + nR_1 (R + R_2)}$$

where $$R_1 = \frac{R}{2^n - 1}$$

and $$R_2 = \frac{R_p}{n(2^{n-1} - 1)}$$

Let $$\frac{E_{bb}}{\Delta E} = F$$

Solve for R_p.

$$R_p = \frac{nR_1\left[R_2 (F - 1) - R\right]}{R + R_1 + R_2}$$

The equivalent circuit of Drawing A-30534 will permit an expression to be obtained for the equivalent load resistance seen by the buffer amplifier, $R_{L(eq)}$.

$$R_{L(eq)} = \frac{nR_1 (R + R_2)}{R + R_1 + R_2}$$

Using the tube characteristics for the tube type selected, draw a line of slope $-1/R_{L(eq)}$ passing through E_{bb} and a line of slope $1/R_p$ passing through the origin. The intersection of the two lines determines the operating point of an "on" buffer amplifier. If this point does not lie in a satisfactory region on the tube characteristics, a different tube must be selected and the design repeated.

Design of an Eight-Position Switch

The known factors are:

1. $n = 3$
2. $\tau_m = 0.5 \mu s$
3. $R_1 = 100,000$ ohms
4. $C_1 = 4.3 \mu\mu f$
5. $\Delta E = 20$ volts

First try an E_{bb} of 100 volts and a 2051 buffer amplifier. The output capacitance of a 2051 is 2.2$\mu\mu$f.

The matrix was constructed and mounted on a cutaway panel so that the other capacitances could be measured. Photograph F55 illustrates the construction of the matrix. The measurements were made just before the crystals were placed in the matrix. The capacitance of a vertical wire of the matrix plus the wire to the tube socket, with all other wires of the matrix grounded, measured 4.5$\mu\mu$f. The capacitance of a horizontal wire of the matrix plus the wire to the tube socket, with all other wires of the matrix grounded, measured 3.3$\mu\mu$f. Also, the interelectrode capacitance of the 1N34 crystal rectifier was measured and found to be approximately 0.5$\mu\mu$f. The capacitance to ground of a crystal rectifier was estimated to be 0.5$\mu\mu$f. Then,

$$C_1 = 0.5\,\mu\mu f$$
$$C_2 = 0.5\,\mu\mu f$$
$$C_3 = 6.7\,\mu\mu f$$
$$C_4 = 7.6\,\mu\mu f$$

Calculating C,

$$C = n(2^{n-1}-1)C_1 + n(C_2 + C_3) + C_4$$
$$= 9(0.5) + 3(7.2) + 7.6$$
$$= 33.7\,\mu\mu f$$

Then, $$R = \frac{T_m}{2.3C}$$

$$= \frac{(0.5)\ (10^6)}{(2.3)\ (33.7)}$$

$$= 6{,}500 \text{ ohms}$$

and, $$R_L = \frac{RR_1}{R_1 - R}$$

$$= \frac{(6{,}500)\ (100{,}000)}{100{,}000 - 6{,}500}$$

$$= 7{,}000 \text{ ohms}$$

If the nearest ten per cent resistor is used,

$$R_L = 6{,}800 \text{ ohms}$$

As may be seen from Drawing A-38201-G, a reasonable value for R_b is 200,000 ohms. Then,

$$R_1 = \frac{R}{2^n - 1}$$

$$= \frac{6{,}500}{7}$$

$$= 930 \text{ ohms}$$

$$R_2 = \frac{R_b}{n(2^n - 1)}$$

$$= \frac{200{,}000}{9}$$

$$= 22{,}200 \text{ ohms}$$

$$F = \frac{E_{bb}}{\triangle E}$$

$$= \frac{100}{20}$$

$$= 5$$

Giving, $$R_p = \frac{nR_1 \left[R_2(F - 1) - R \right]}{R + R_1 + R_2}$$

$$= \frac{(3)\ (930) \left[(22,200)\ (4) - 6,500 \right]}{6,500 + 930 + 22,200}$$

$$= 7,750 \text{ ohms}$$

and, $$R_{L(eq)} = \frac{nR_1\ (R + R_2)}{R + R_1 + R_2}$$

$$= \frac{(3)\ (930)\ (6,500 + 22,200)}{6,500 + 930 + 22,200}$$

$$= 2,700 \text{ ohms}$$

The plate characteristic of the 2C51 is shown in Drawing A-38202-G. The operating point is shown at the intersection of the two lines determined by R_p, $R_{L(eq)}$ and E_{bb}. The operating point is seen to lie below both the maximum-plate-dissipation curve, 0.75 watt, and the maximum-cathode-current line, 18 milliamperes. The curves also show that the grid of the buffer amplifier must be driven to about +0.5 volt.

Note that the plate dissipation of an "on" buffer

amplifier in the eight-position switch just designed is about 0.75 watt. Next, a thirty-two position switch will be designed to the same specifications. The following design will show that transmitting tubes are necessary to achieve the same performance in a thirty-two position switch.

Design of a Thirty-Two-Position Switch

The known factors are:

1. $n = 5$
2. $\tau_m = 0.5 \mu s$
3. $R_1 = 100{,}000$ ohms
4. $C_1 = 4.3 \mu\mu f$
5. $\triangle E = 20$ volts

Try an E_{bb} of 100 volts and an 829-B buffer amplifier with a screen voltage of 200 volts. The output capacitance of an 829-B is 7 $\mu\mu f$. Estimates of the shunt capacitances may be based upon the measurement made on the eight-position matrix, giving

$C_1 = 0.5 \mu\mu f$

$C_2 = 0.5 \mu\mu f$

$C_3 = 25 \mu\mu f$

$C_4 = 9.3 \mu\mu f$

Calculating C,

$$C = n(2^{n-1}-1)\, C_1 + n(C_2 + C_3) + C_4$$

$$= 75(0.5) + 5(25.5) + 9.3$$

$$= 174.3 \mu\mu f$$

Then,

$$R = \frac{T_m}{2.30}$$

$$= \frac{(0.5)\ (10^6)}{(2.3)\ (174.3)}$$

$$= 1{,}250 \text{ ohms}$$

and,

$$R_L = \frac{RR_1}{R_1 - R}$$

$$= \frac{(1{,}250)\ (100{,}000)}{100{,}000 - 1{,}250}$$

$$= 1{,}270 \text{ ohms}$$

As in the preceding design, R_b will be taken as 200,000 ohms. Then,

$$R_1 = \frac{R}{2^n - 1}$$

$$= \frac{1{,}250}{31}$$

$$= 40.4 \text{ ohms}$$

$$R_2 = \frac{R_b}{n(2^{n-1}-1)}$$

$$= \frac{200{,}000}{75}$$

$$= 2{,}670 \text{ ohms}$$

$$F = \frac{E_{bb}}{\Delta E}$$

$$= \frac{100}{20}$$

$$= 5$$

Giving, $$R_p = \frac{nR_1[R_2 (F - 1) - R]}{R + R_1 + R_2}$$

$$= \frac{(5)\ (40.4)\ [(2,670)\ (4) - 1,250]}{1,250 + 40.4 + 2,670}$$

$$= 478 \text{ ohms}$$

and $$R_{L(eq)} = \frac{nR_1\ (R + R_2)}{R + R_1 + R_2}$$

$$= \frac{(5)\ (40.4)\ (1,250 + 2,670)}{1,250 + 40.4 + 2,670}$$

$$= 198 \text{ ohms}$$

The operating point, as determined from the published characteristics for the 829-B is at the point where

E_b = 72 volts

I_b = 150 ma.

E_{cl} = -2 volts

The plate dissipation of an "on" buffer amplifier is then 10.6 watts. The rated plate dissipation for the 829-B is 15 watts.

The foregoing two designs illustrate the large increase in the power required to drive a matrix as the number of terminals is increased. The power required goes up for two reasons: first, the matrix becomes larger increasing the shunt capacitance; second, the equivalent load resistance for the buffer amplifiers goes down because the tubes must draw current thru more R's in parallel.

EXPERIMENTAL VERIFICATION OF THE ANALYSIS

The eight-position switch designed in the previous section was constructed and its performance determined experimentally. The experiments will be described in this section.

The crystal rectifiers were soldered into the matrix as shown in Photograph F55. Before the buffer amplifiers were connected to the matrix, the equivalent load resistance for the buffer amplifiers, $R_{L(eq)}$, was determined using the circuit of Drawing A-30549.

$$R_{L(eq)} = \frac{2E}{I}$$

The resistance $R_{L(eq)}$ was found to vary from 2,880 ohms at an E of 5 volts to 2,770 ohms at an E of 25 volts. This checks well with the calculated value of 2,700 ohms. The measured resistance is higher because the forward resistance of the rectifiers was neglected in the calculation of $R_{L(eq)}$; and, the measured resistance decreases with increasing voltage because the resistance of the rectifiers decreases with increasing forward current.

The 2051 buffer amplifiers were connected to the matrix as shown in Drawing A-30550. The grids of three of the buffer amplifiers were connected to the cathodes and the other three grids were connected to a voltage far below cutoff. The voltages at the plates of the buffer amplifiers and the terminals of the matrix are

indicated on the drawing. The voltage of the selected terminal is -2.7 volts. The voltage of the non-selected terminals ranges from -24.5 to -24.8 volts. Then ΔE is 22 volts, which checks well with the calculated value of 20 volts. The difference may be explained by the fact that the actual static plate resistance for the 2051's is lower than that determined from the published characteristics.

The previous two experiments verify the static analysis. The next step is to examine the dynamic analysis.

Drawing A-30551 shows the circuit used to check the dynamic behavior. The buffer amplifiers are connected so that the application of a positive rectangular pulse and a negative rectangular pulse at the indicated terminals will produce the same effect as setting all three flip-flops at the beginning of the pulse and resetting all the flip-flops at the end of the pulse. The advantage of using a pulse generator rather than using three flip-flops is that much faster rise and fall times may be obtained from a gas-tube pulse generator; the buffer amplifiers may be assumed to switch on or off instantaneously and simultaneously.

The block diagram of the complete experiment is shown in Drawing A-30552. The Model 5 Synchroscope delivers trigger pulses to the pulse generator at a 1000-cps pulse-repetition frequency. Photographs of the negative and positive pulses produced by the pulse generator are shown in Drawing A-30553. The waveforms at all eight terminals are also shown. Initially, terminal 0 is the selected

terminal. During the pulse, terminal 7 is selected and the voltage at terminal 0 drops to the normal non-selected voltage. After the pulse, terminal 0 returns to the selected voltage and terminal 7 drops to the non-selected voltage. The ΔE is 20 volts, or 4.2 divisions. The pulse is one microsecond long, or 12 divisions. The voltage at terminal 0 reaches 10 per cent of ΔE of its final value in about 0.1 microsecond. The transients at the non-selected terminals subside at the same time. At terminal 7, the terminal being selected, the voltage reaches 10 per cent of ΔE of its final value in 0.65μs, a fair check with the calculated τ_m of 0.5μs. However, the long portion of the transient at terminal 7 indicates a time consistant of 0.35μs, measured graphically, or an effective shunt capacitance of 54$\mu\mu$f. This must be compared with the estimated shunt capacitance, 33.7$\mu\mu$f. The difference may be attributed to the following factors: error in the graphical measurement, experimental factors such as the additional capacitance added by the deflection plates, and an error in the original estimate of the shunt capacitance. The last factor is believed to be the most important. The discrepancy is not believed to be the fault of the dynamic analysis because the performance of the switch checks in other respects very well with that expected. The assumption important to the concept of a shunt capacitance, that the other parts of the switch be considered at a fixed potential, is seen to be valid: the experimental waveforms show no change in voltage of the other parts of the switch during the long portion of the transient at terminal 7.

Flip-flops were designed and added to the matrix so that it could be operated as a true switch. The circuit diagram of one of the flip-flops is shown in Drawing A-30554. The drawing also shows the method of coupling the flip-flop to the buffer amplifiers. The reset terminals of the three flip-flops were tied to a common point so that all three flip-flops could be reset by a single pulse. Note that the flip-flop holds the grid of an "on" buffer amplifier 0.6-volt positive with respect to the cathode. The selected terminal in this case is at -4.0 volts and the voltage of the non-selected terminals ranges from -30.3 to -30.8 volts, giving a ΔE of 26.3 volts. The switch tested is shown in Photographs F56 and F53.

The block schematic for testing the eight-position switch is shown in Drawing A-30555. The arrangement for testing the switch is also shown in Photograph F58. As before, the Model 5 Synchroscope is cynchronized at a 1000-cps pulse-repetition frequency. Pulses from the synchroscope trigger the gas-tube pulse generator which produces negative pulses 0.2-microsecond long and 50-volts amplitude. The pulses are attenuated to 8 volts amplitude by the attenuator, shown in the foreground of Photograph F28. The attenuated pulses are used to set the flip-flops. The coding switches, immediately above the attenuator in the photograph, permit the selection of any terminal. The attenuated pulses, delayed one microsecond by a delay line, also reset the switch to the zero position.

The waveforms at the zero terminal, a non-selected terminal, and the selected terminal are shown for the three basic types of

transitions in Drawing A-30556. The differences between the waveforms of Drawing A-30553 and Drawing A-30556 are due to the switching time of the flip-flops, corresponding to the time interval $t_2 - t_1$. The waveforms have the characteristics predicted by the analysis. For example, the temporary final value to which the non-selected terminals charge is a fraction of $\triangle E$ for the first type of transition, a larger fraction of $\triangle E$ for the second type of transition, and the entire $\triangle E$ for the third type of transition. The voltage and time scales are the same as before, 0.48 volts per division and 0.12 microsecond per division.

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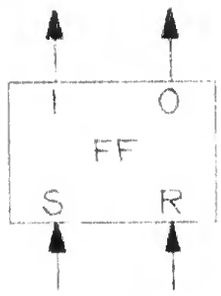
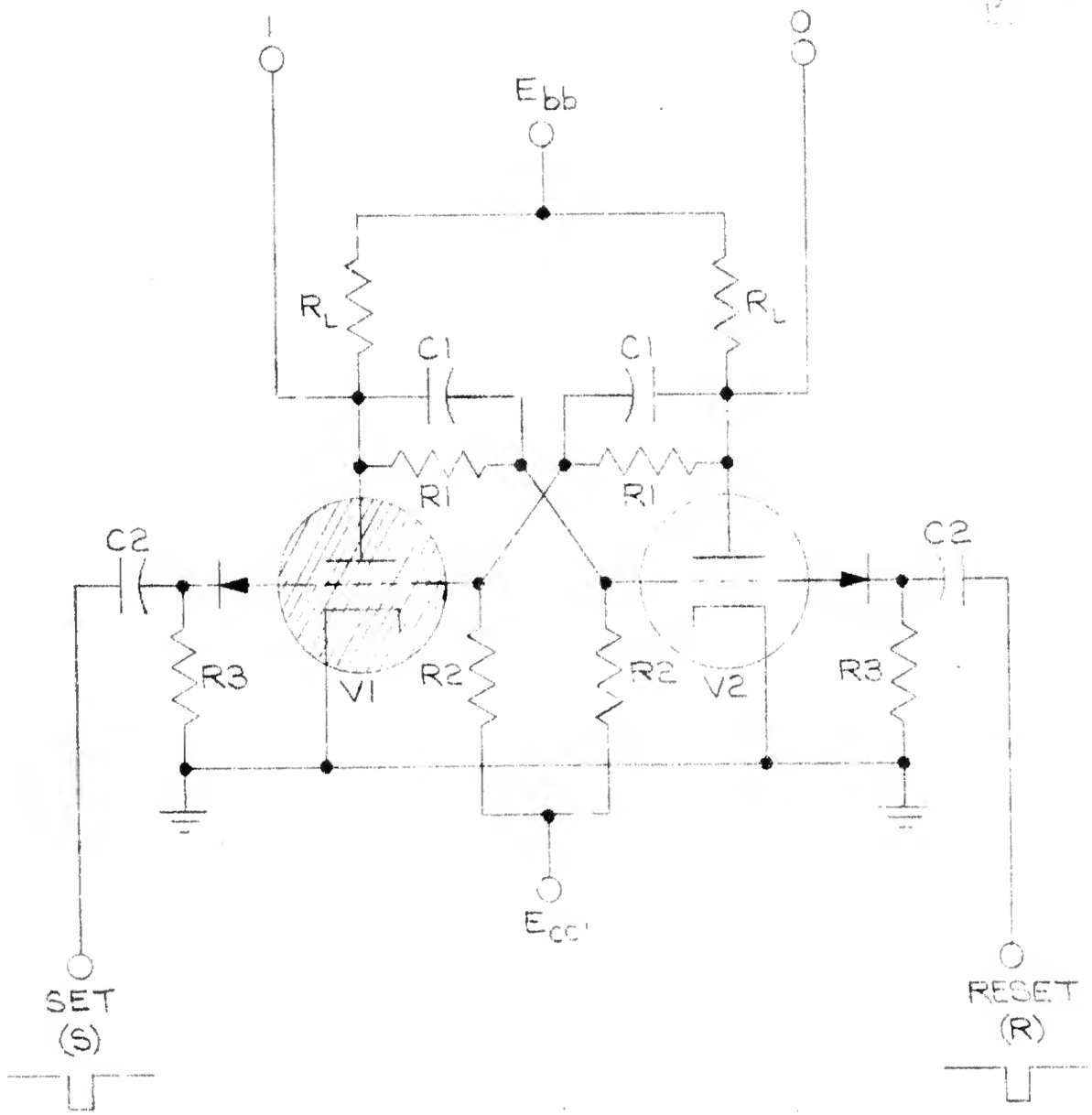
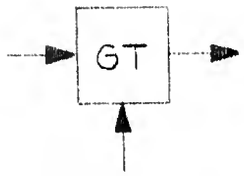
LIST OF PHOTOGRAPHS



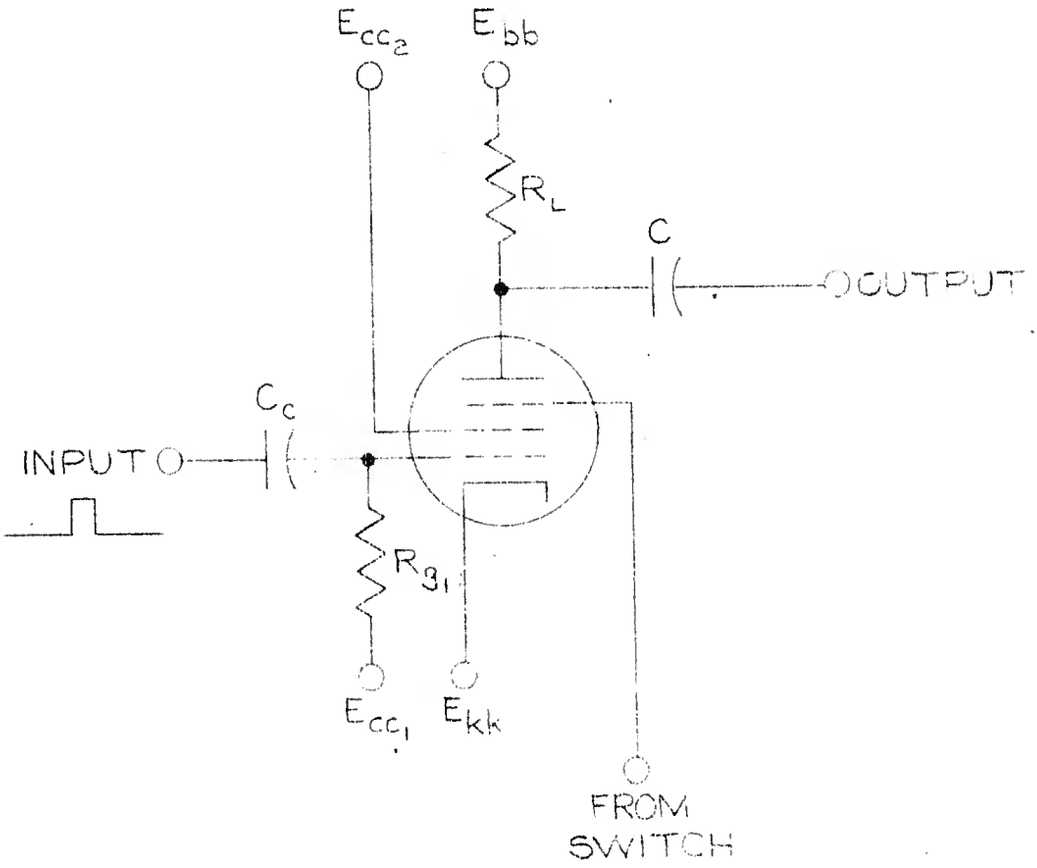
SYMBOL FOR A FLIP-FLOP



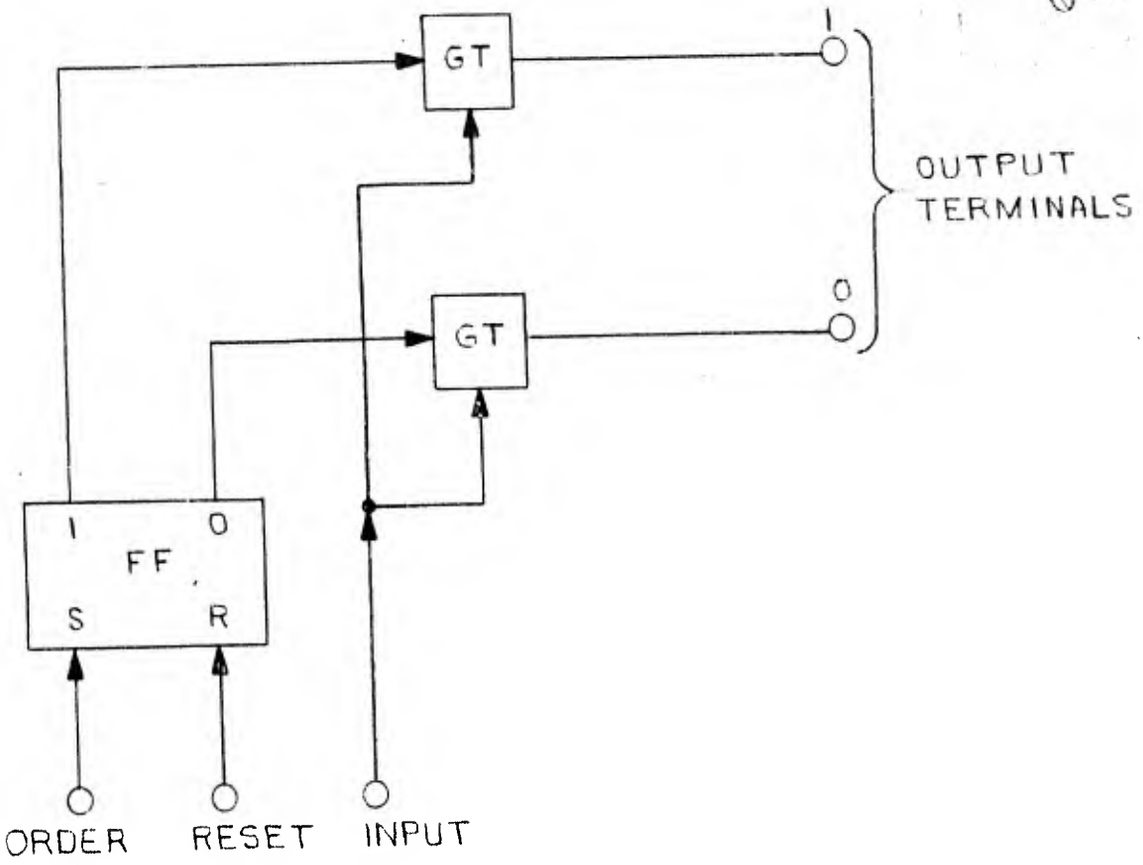
CIRCUIT DIAGRAM OF A
FLIP-FLOP



SYMBOL FOR A
GATE CIRCUIT

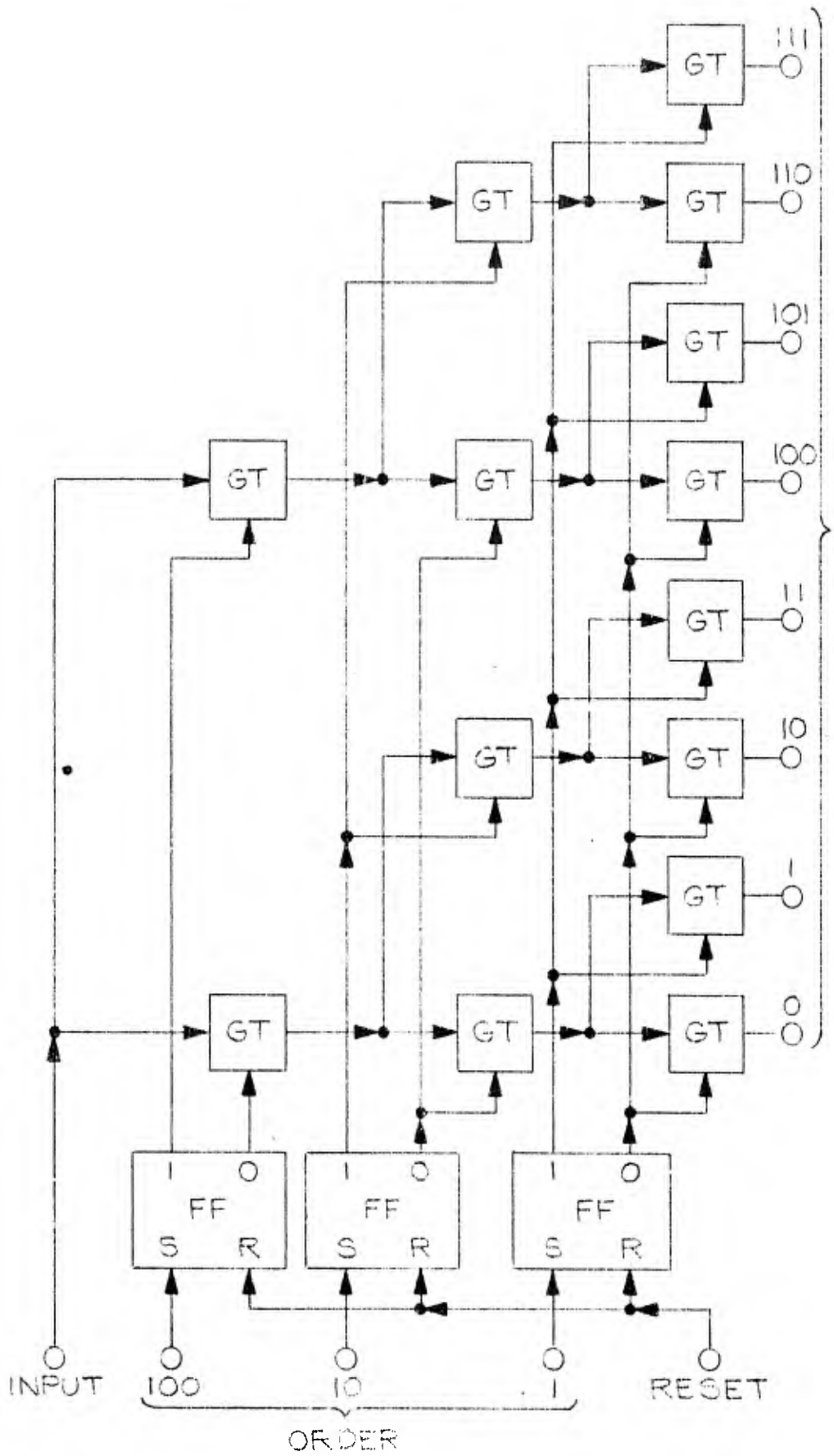


CIRCUIT DIAGRAM OF A
GATE CIRCUIT

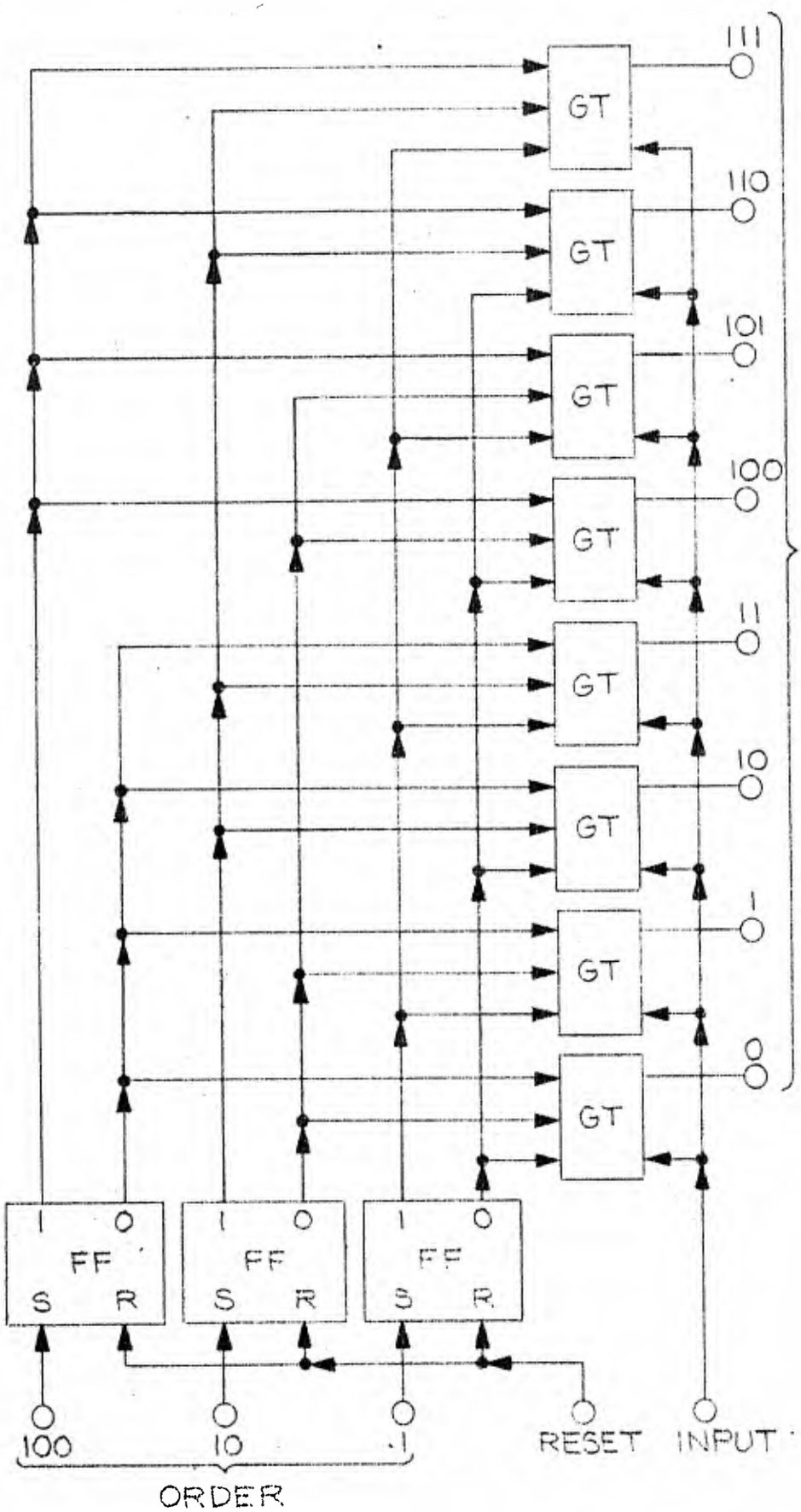


TWO-POSITION SWITCH WITH TWO
OUTPUT CHANNELS

USED IN D.R.B. THESIS

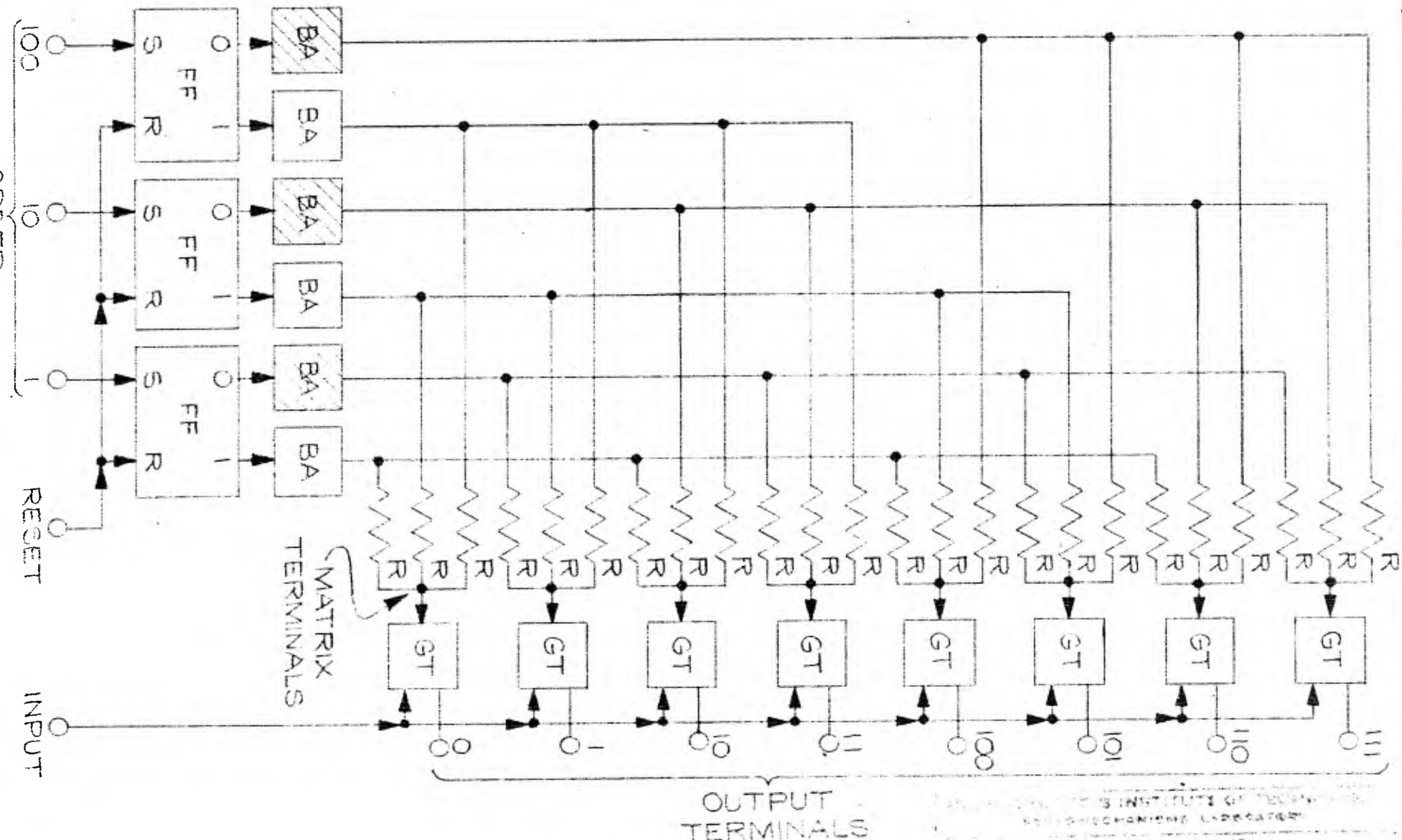


WHIFFLE-TREE GATE-TUBE SWITCH

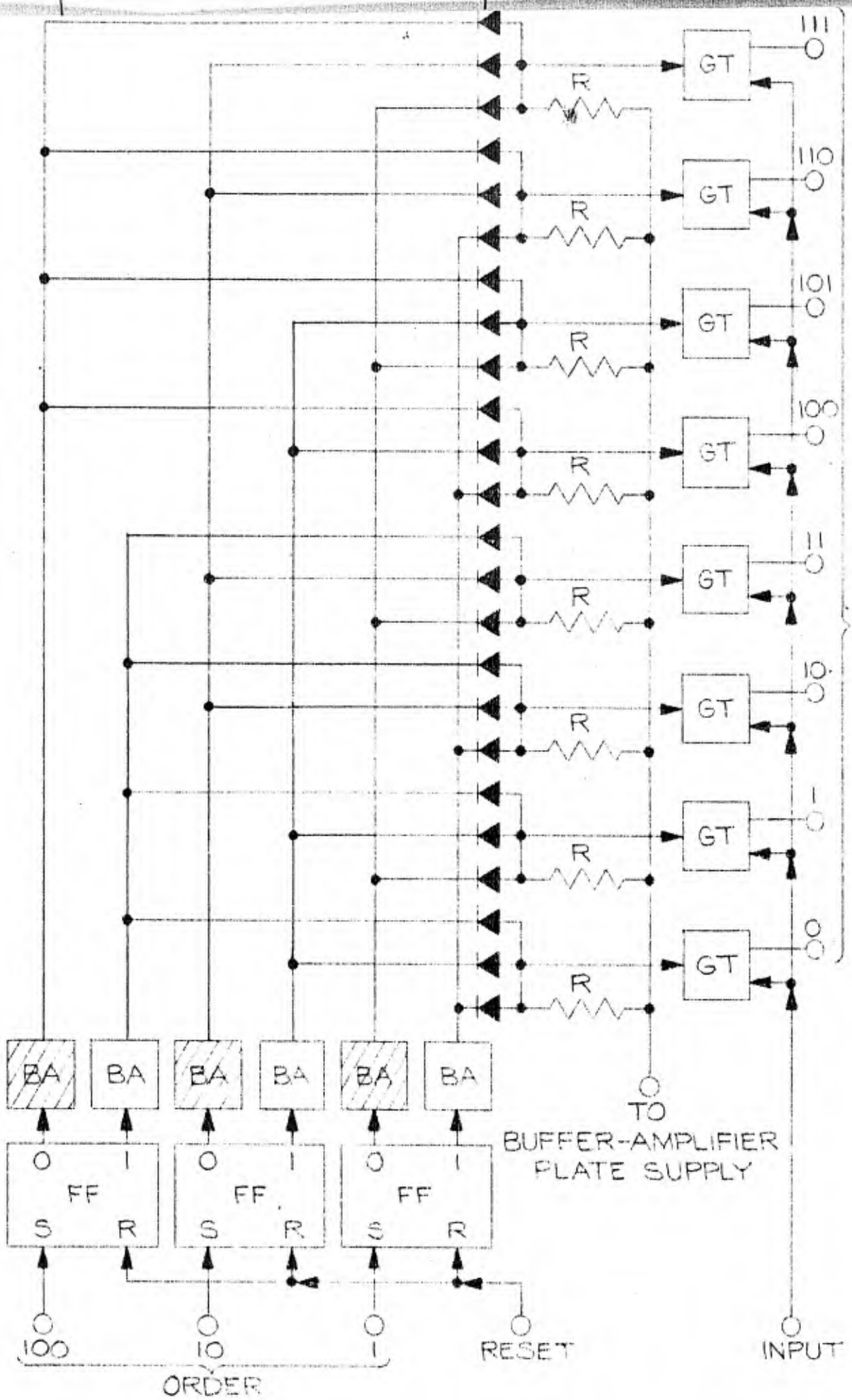


MULTI-GRID GATE-TUBE SWITCH

A-30525-1



6345 DE TI 5/10/47
D.R.B. A-30525-1



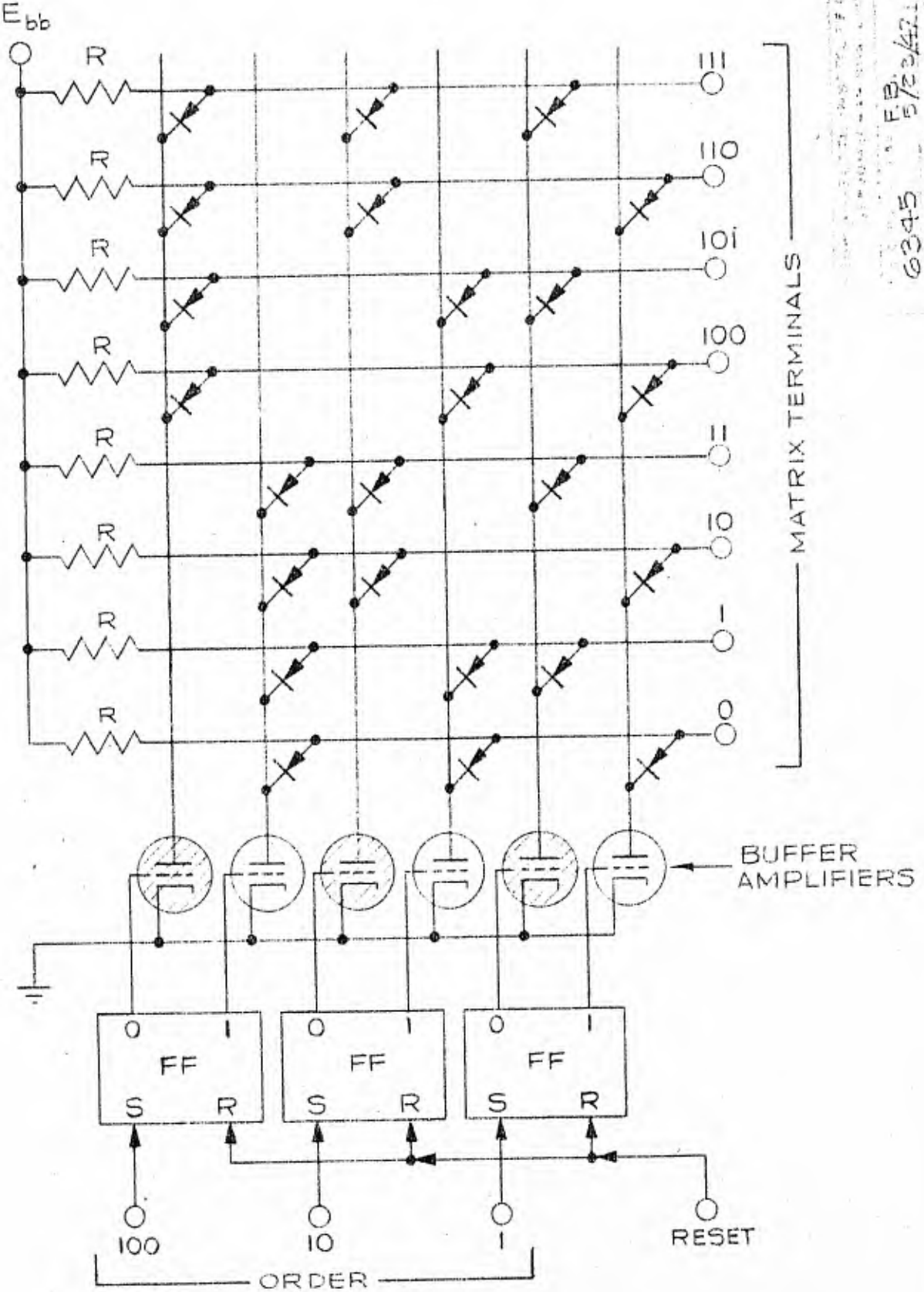
CRYSTAL-MATRIX SWITCH

USED IN D.R.B. THESIS

A-30526-1

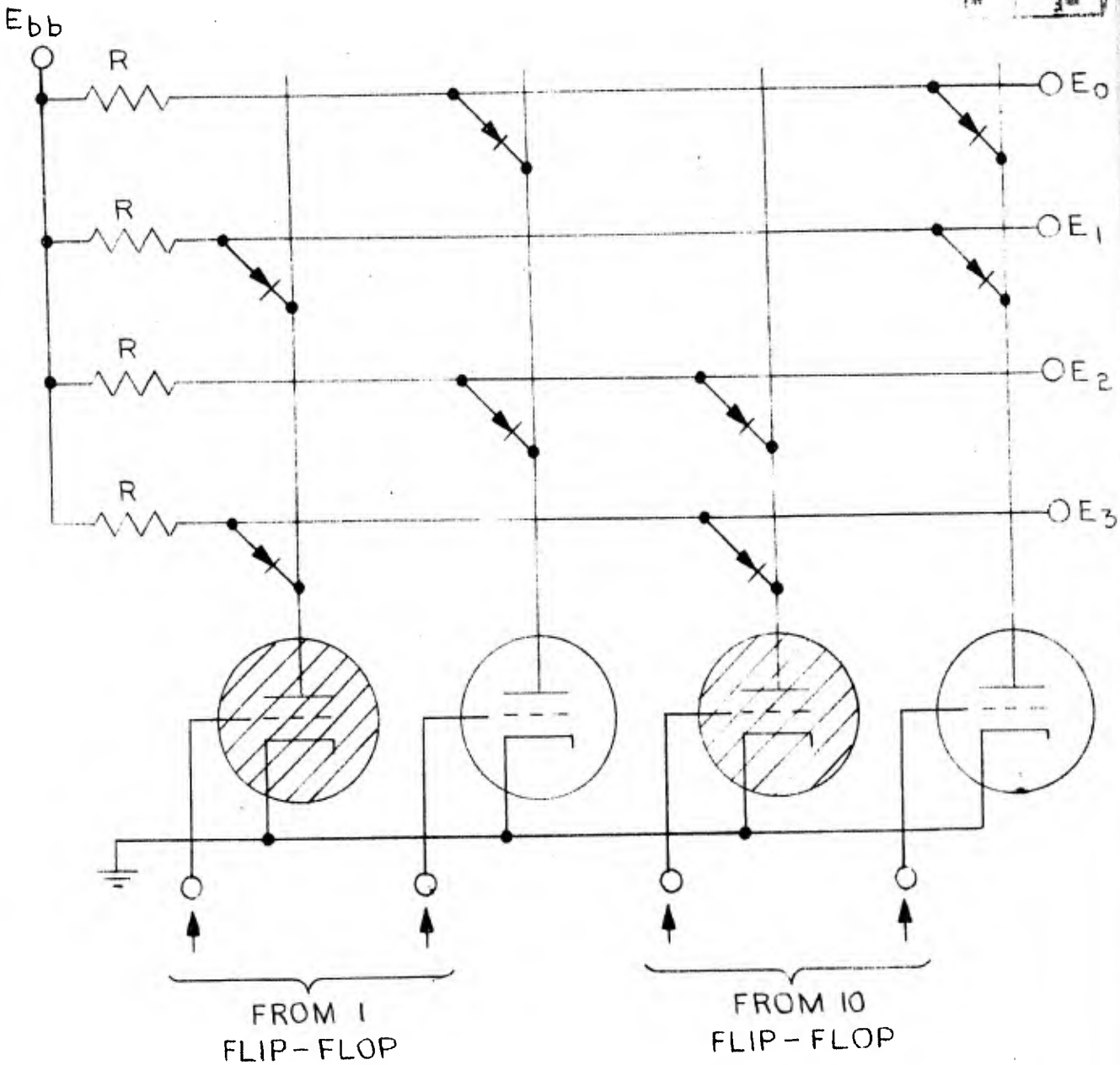
6345 5/12/47 A-30526-1

D.R.B.



CRYSTAL-MATRIX SWITCH REDRAWN

A-30527

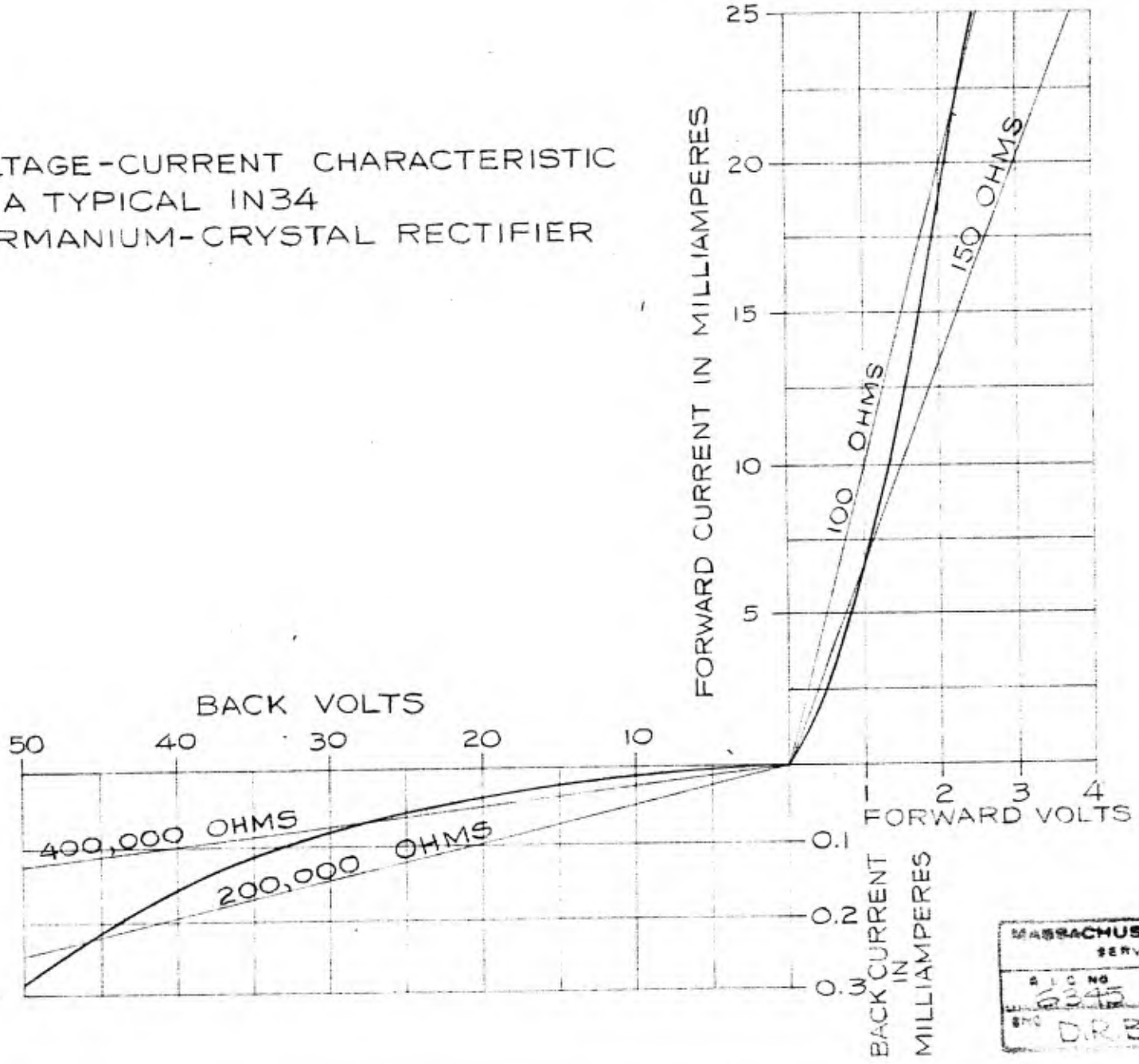


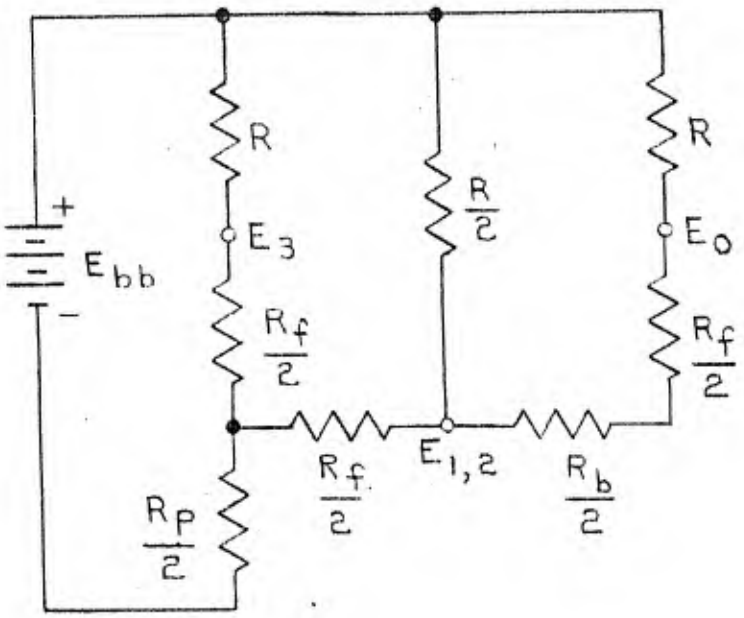
CIRCUIT DIAGRAM OF A FOUR-POSITION
CRYSTAL-MATRIX SWITCH

A-30528

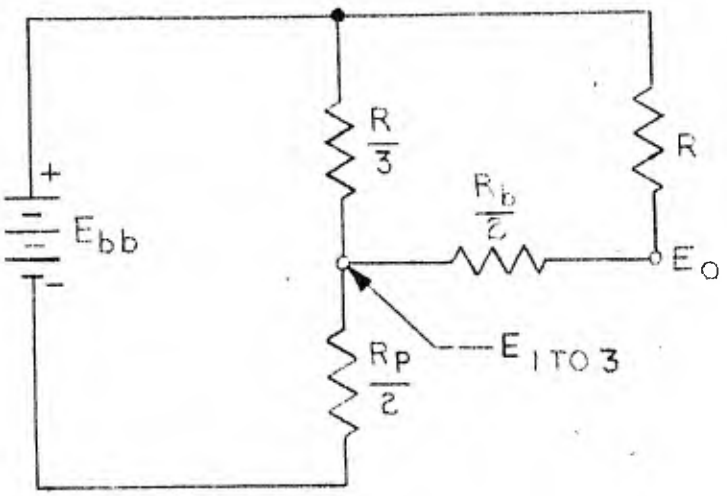
A-38201-G

VOLTAGE-CURRENT CHARACTERISTIC
OF A TYPICAL IN34
GERMANIUM-CRYSTAL RECTIFIER



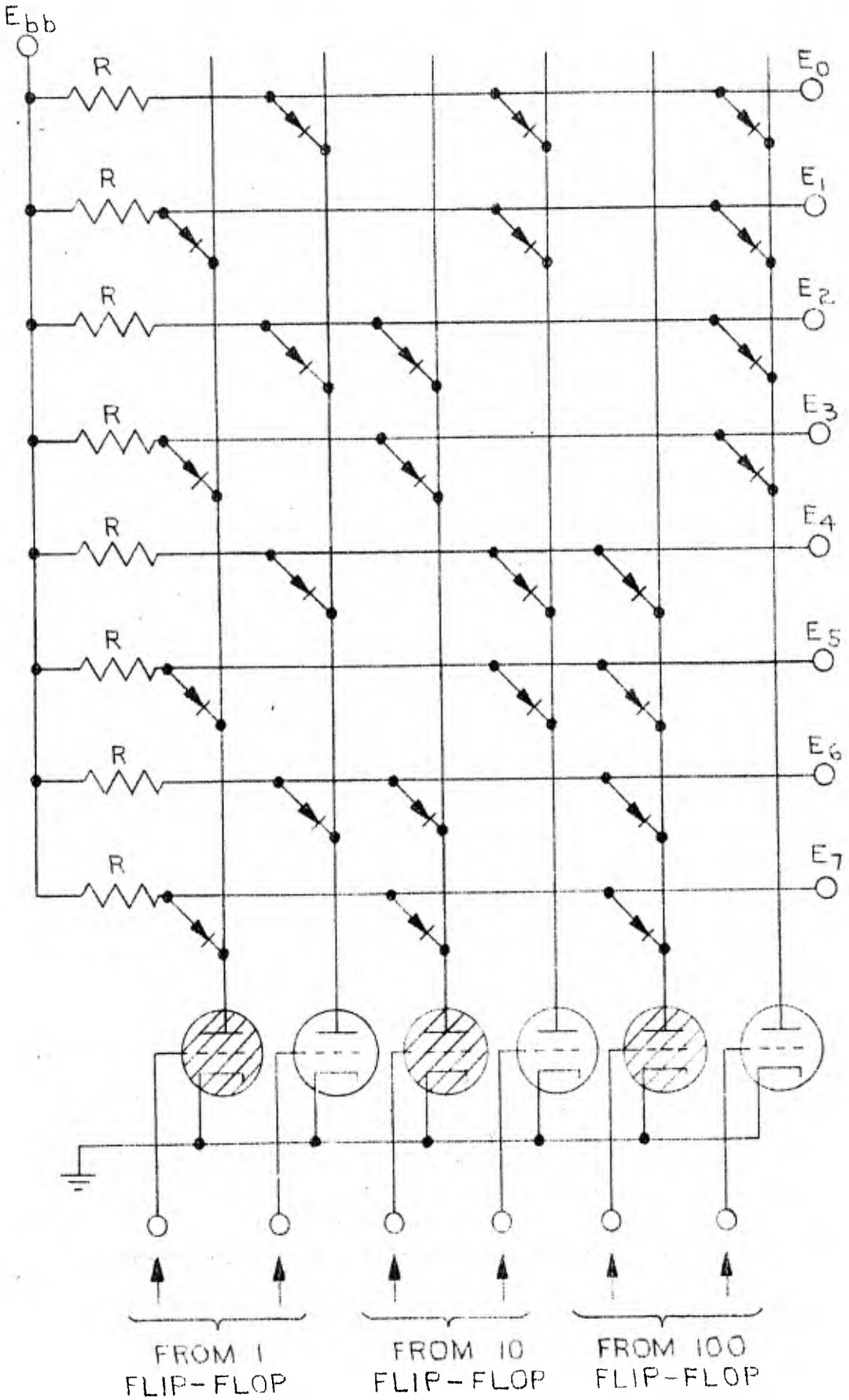


EQUIVALENT CIRCUIT OF THE FOUR-POSITION SWITCH

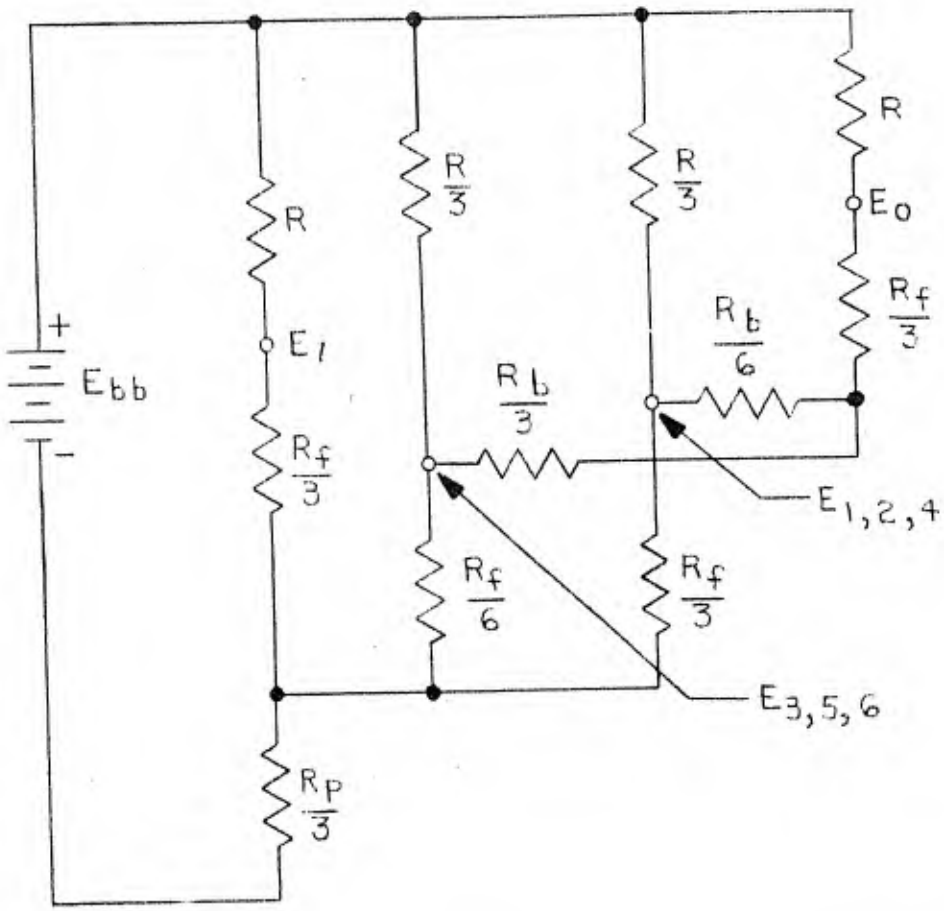


SIMPLIFIED EQUIVALENT CIRCUIT OF THE FOUR-POSITION SWITCH

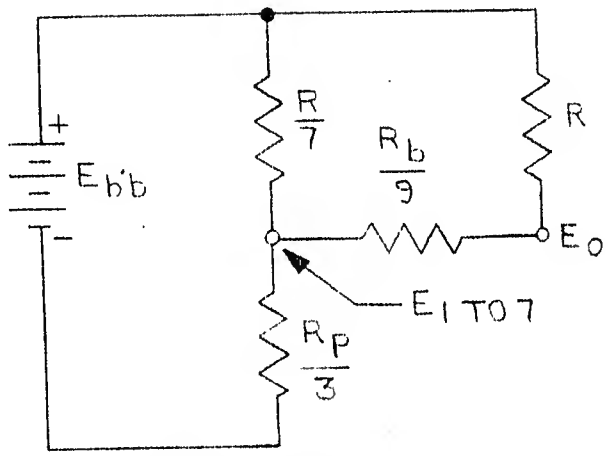
EQUIVALENT CIRCUITS FOR THE FOUR-POSITION SWITCH



CIRCUIT DIAGRAM OF AN EIGHT-POSITION CRYSTAL-MATRIX SWITCH

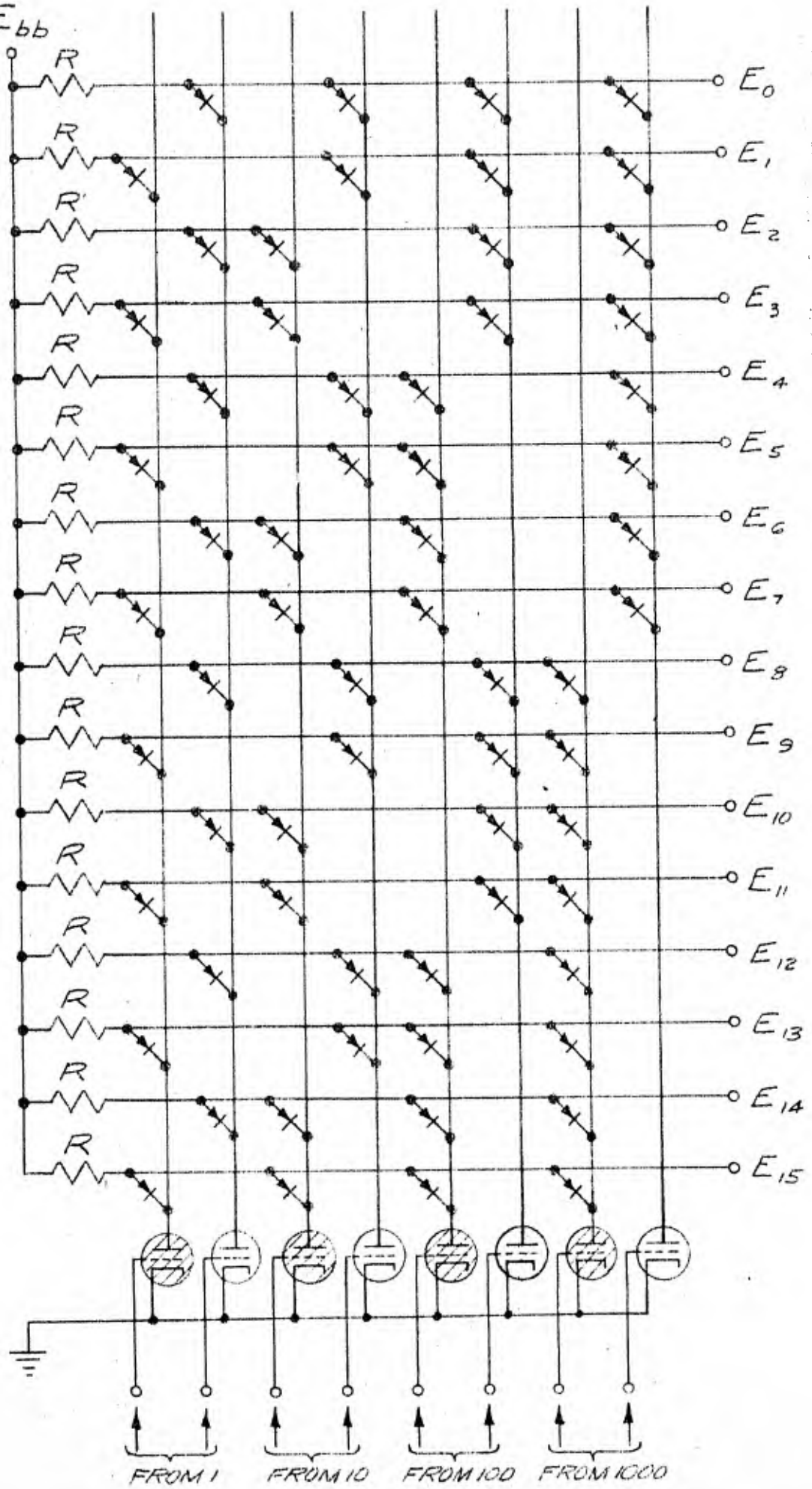


EQUIVALENT CIRCUIT OF THE EIGHT-POSITION SWITCH



SIMPLIFIED EQUIVALENT CIRCUIT OF THE EIGHT-POSITION SWITCH

EQUIVALENT CIRCUITS FOR THE EIGHT-POSITION SWITCH

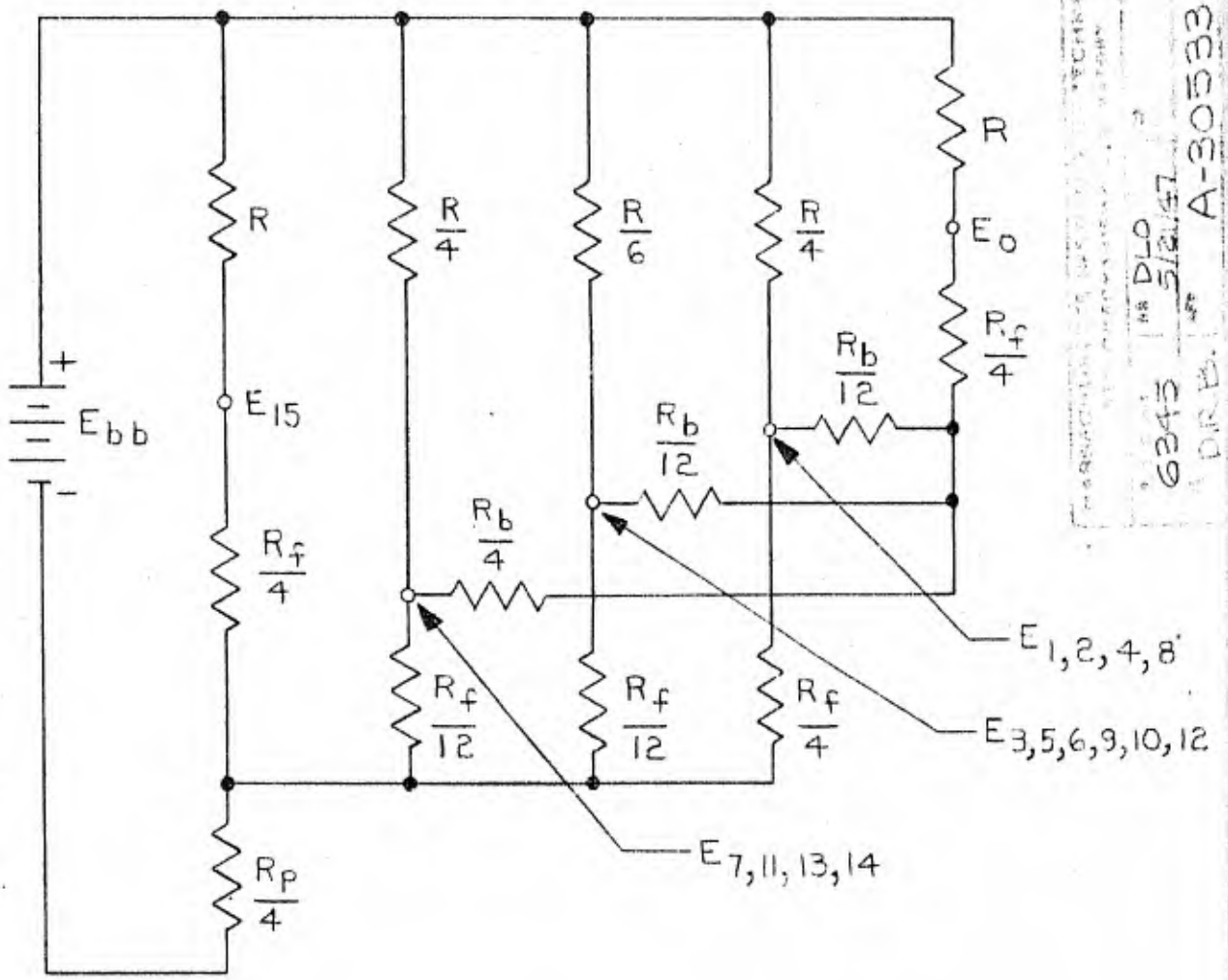


CIRCUIT DIAGRAM OF A SIXTEEN-POSITION CRYSTAL-MATRIX SWITCH

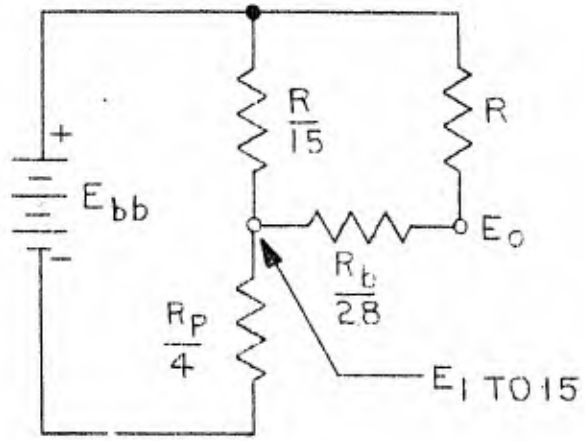
6845 A-30532

D.R.P.

A-30532

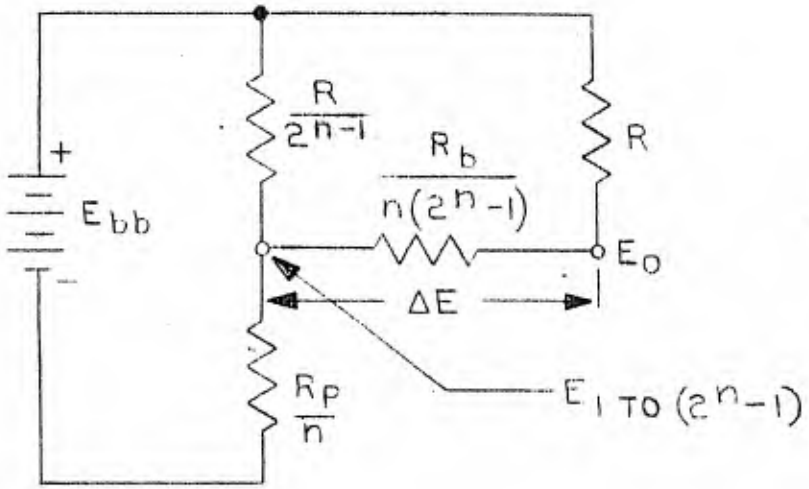


EQUIVALENT CIRCUIT OF THE SIXTEEN-POSITION SWITCH

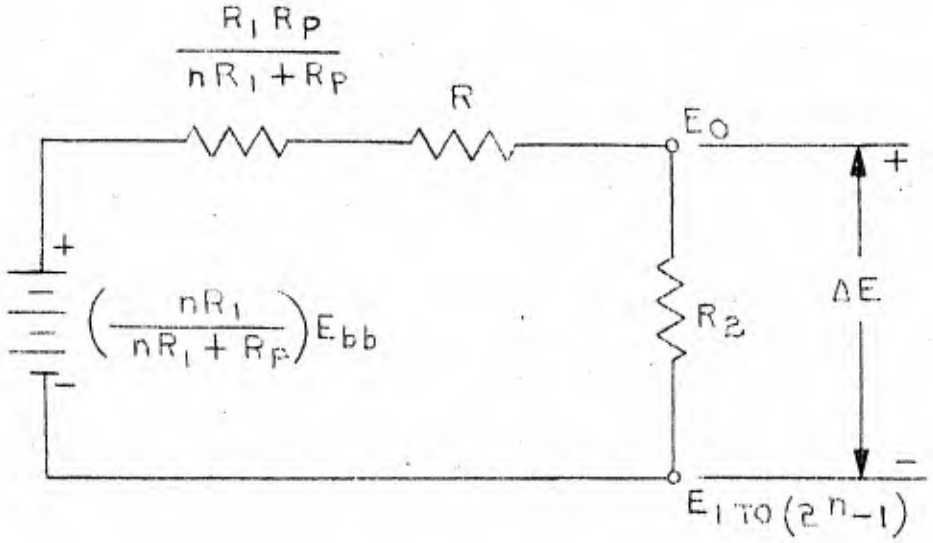


SIMPLIFIED EQUIVALENT CIRCUIT OF THE SIXTEEN-POSITION SWITCH

EQUIVALENT CIRCUITS FOR THE SIXTEEN-POSITION SWITCH

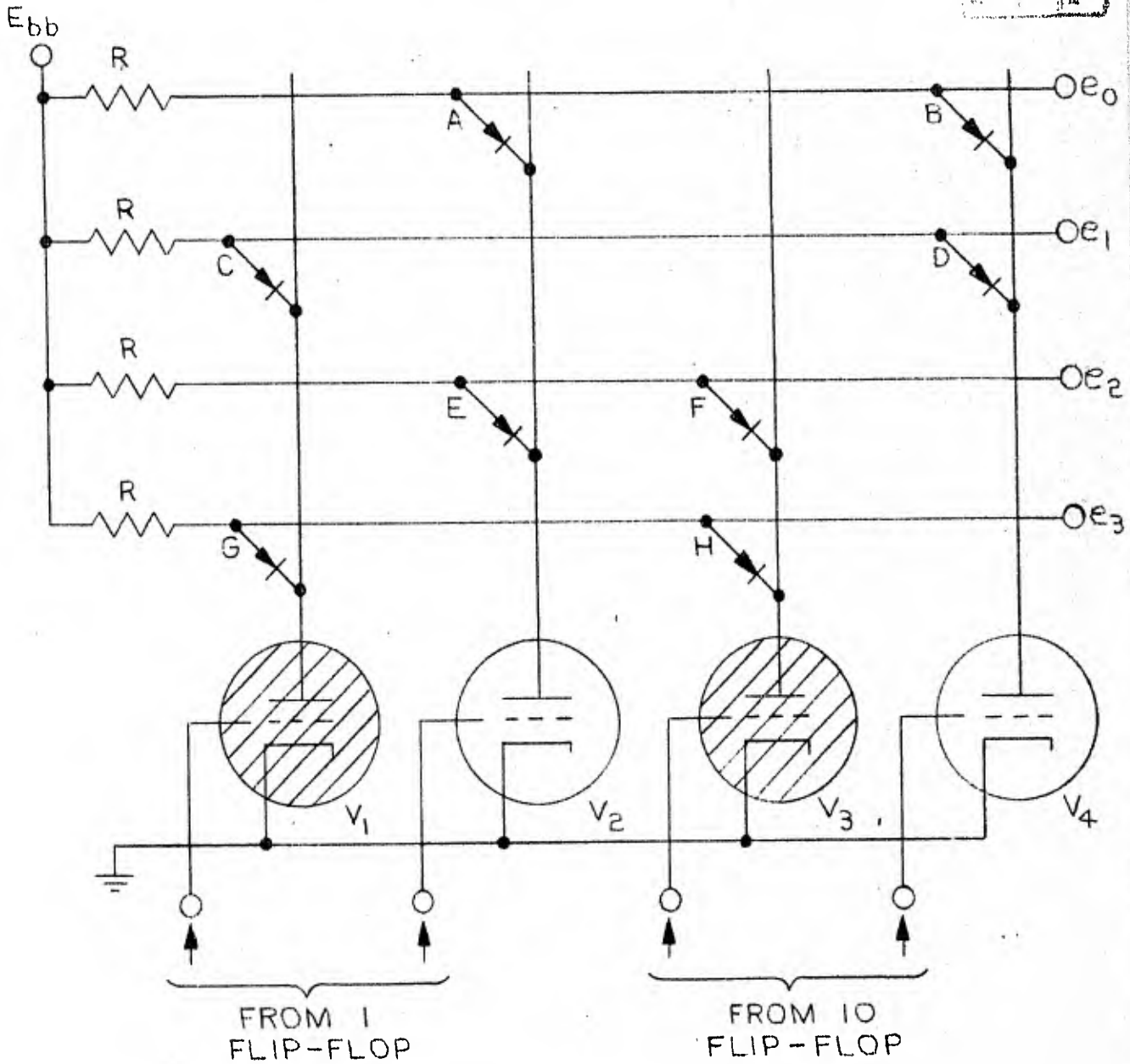


SIMPLIFIED EQUIVALENT CIRCUIT OF THE 2^n - POSITION SWITCH



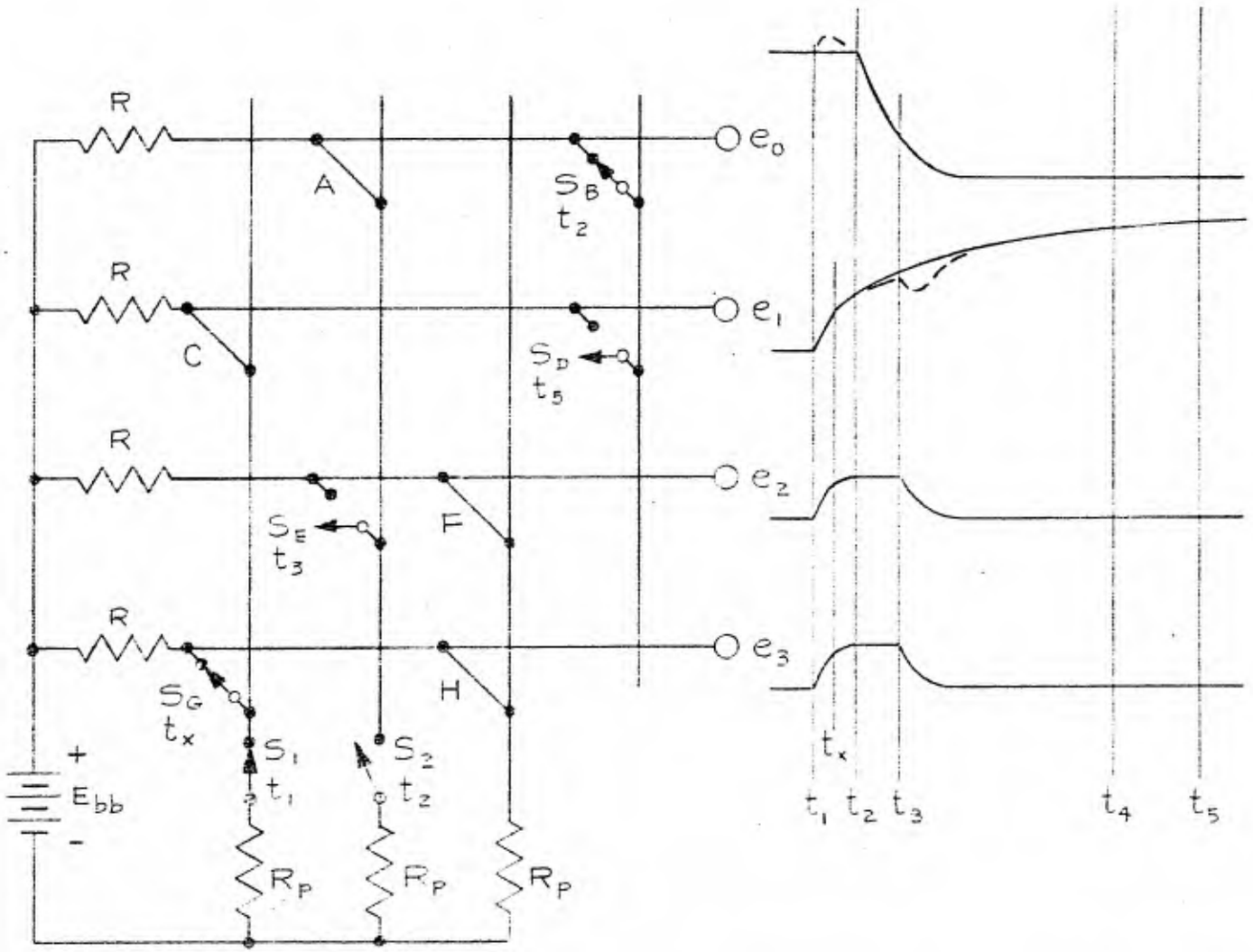
CIRCUIT FOR CALCULATION OF ΔE

EQUIVALENT CIRCUITS FOR THE 2^n-POSITION SWITCH



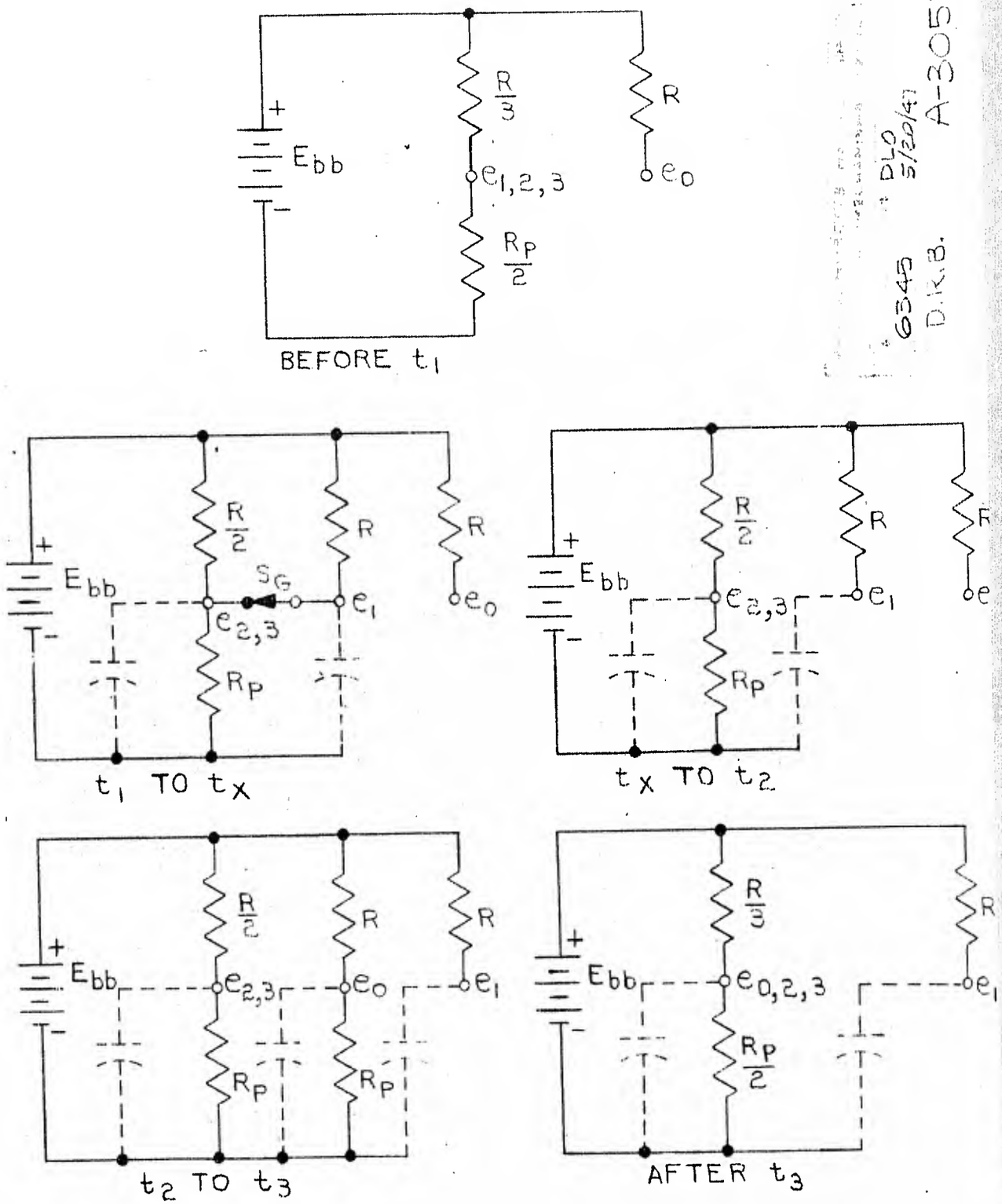
CIRCUIT DIAGRAM OF THE FOUR-POSITION
CRYSTAL-MATRIX SWITCH

A-30536



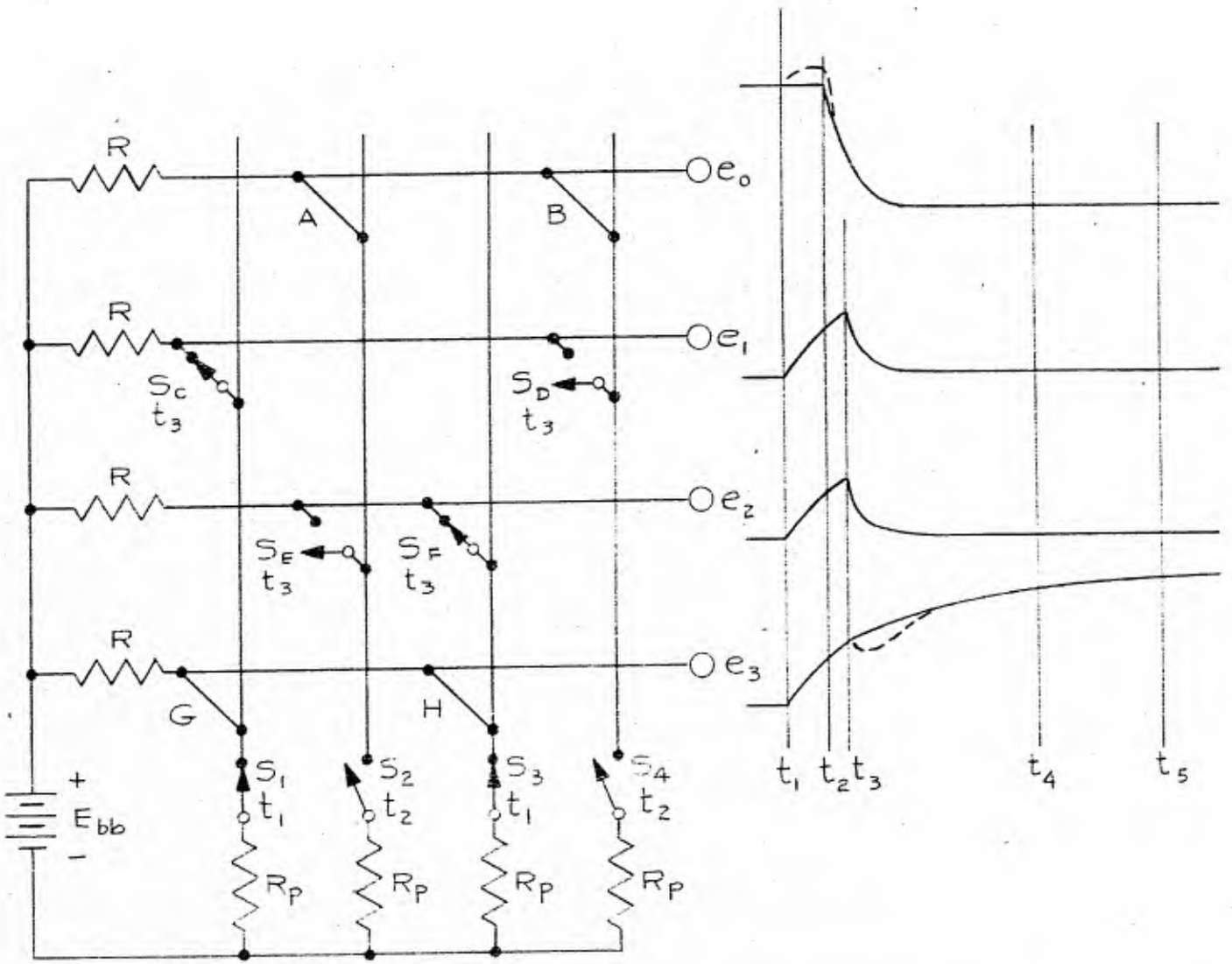
EQIVALENT CIRCUIT FOR THE FOUR-POSITION SWITCH FOR A TRANSITION FROM TERMINAL 0 TO TERMINAL 1

6345 FB. 5/22/47
D.R.B. A-30536

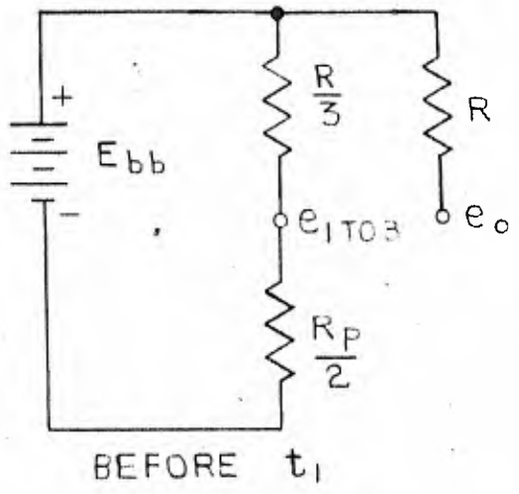


EQUIVALENT CIRCUITS FOR THE FOUR-POSITION SWITCH
FOR A TRANSITION FROM
TERMINAL 0 TO TERMINAL 1

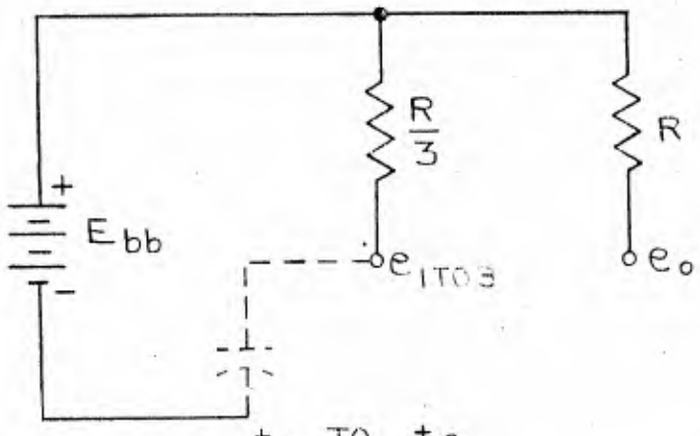
A-30538



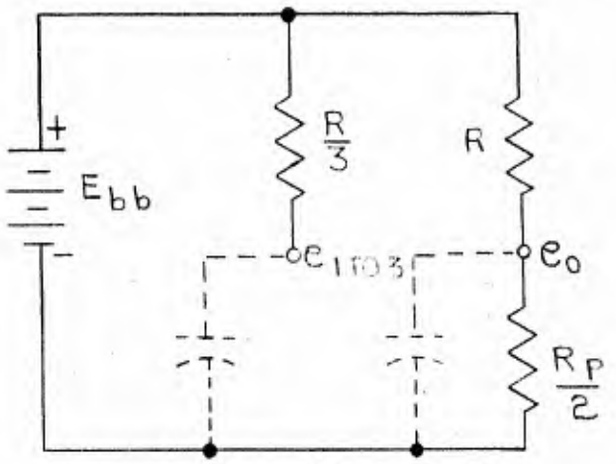
EQIVALENT CIRCUIT FOR THE FOUR-POSITION SWITCH FOR A TRANSITION FROM TERMINAL 0 TO TERMINAL 3



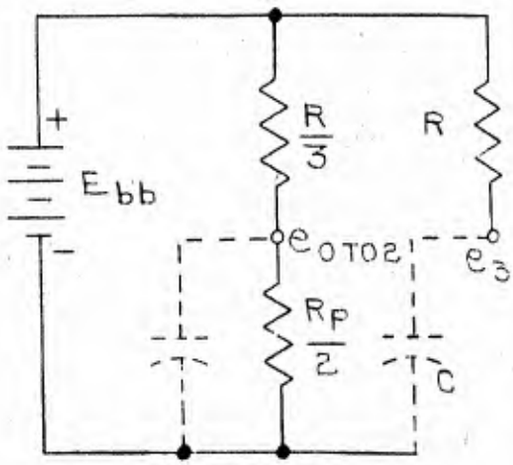
BEFORE t_1



t_1 TO t_2



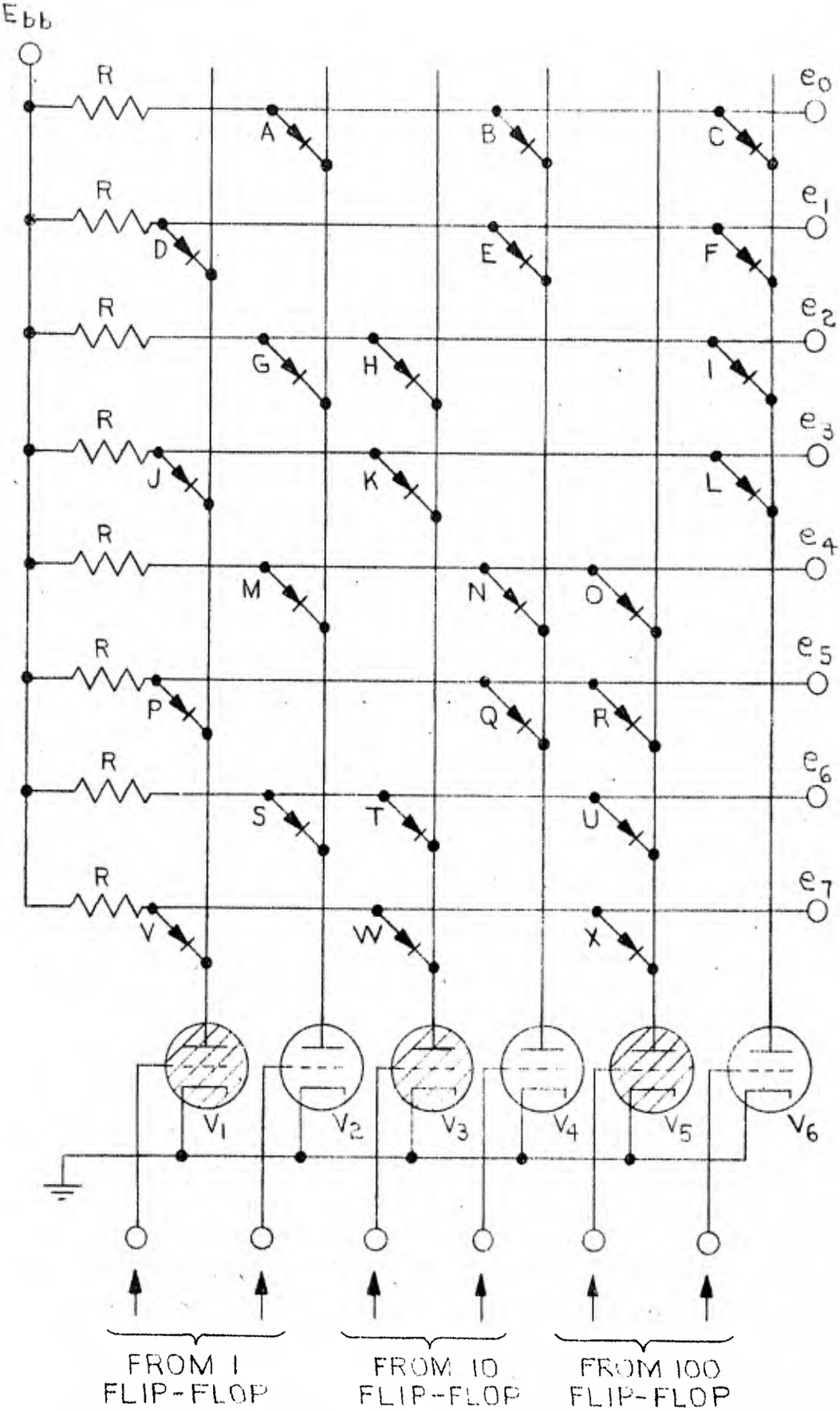
t_2 TO t_3



AFTER t_3

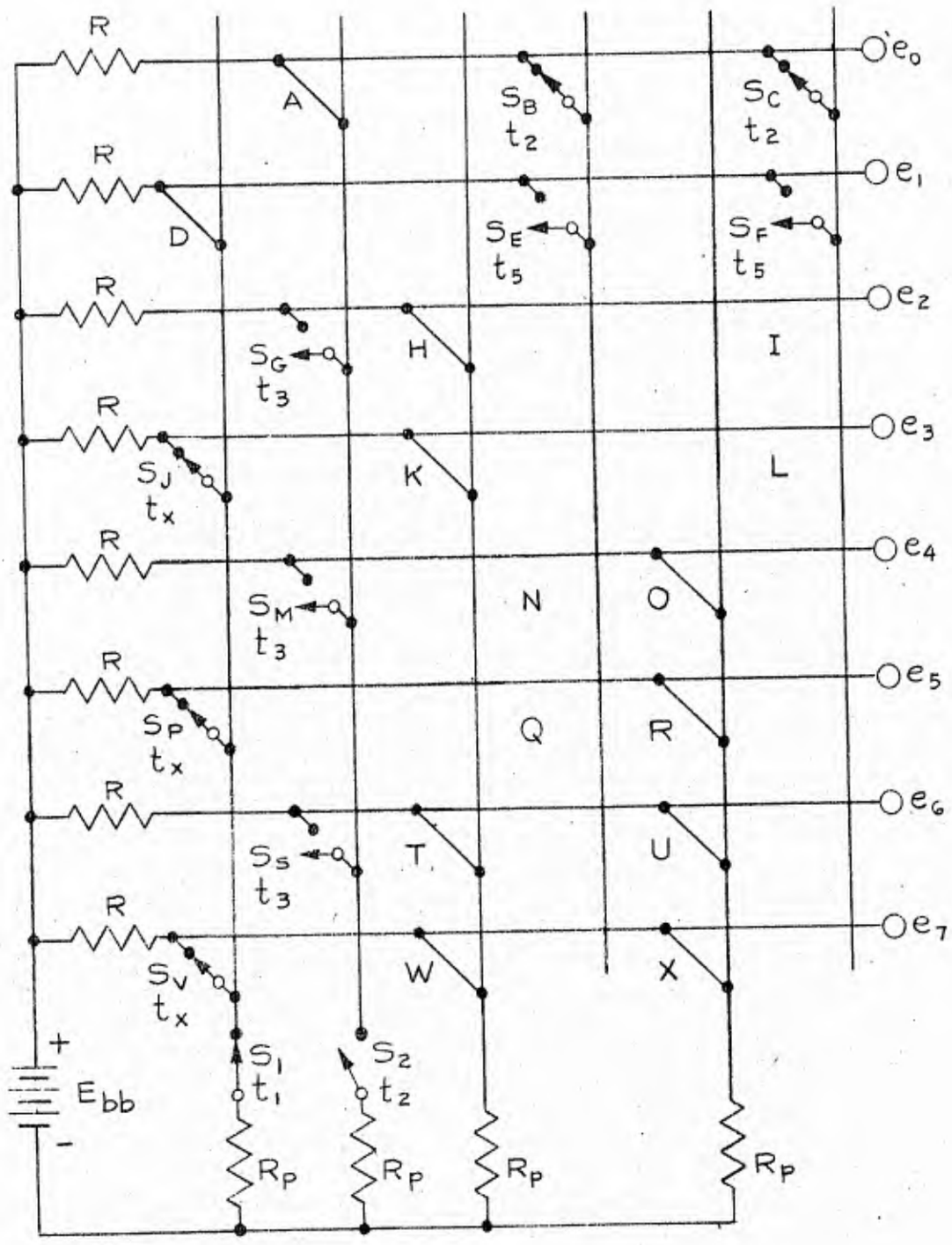
EQUIVALENT CIRCUITS FOR THE FOUR-POSITION SWITCH FOR A TRANSITION FROM TERMINAL O TO TERMINAL 3.

USED IN D.R.B. THESIS

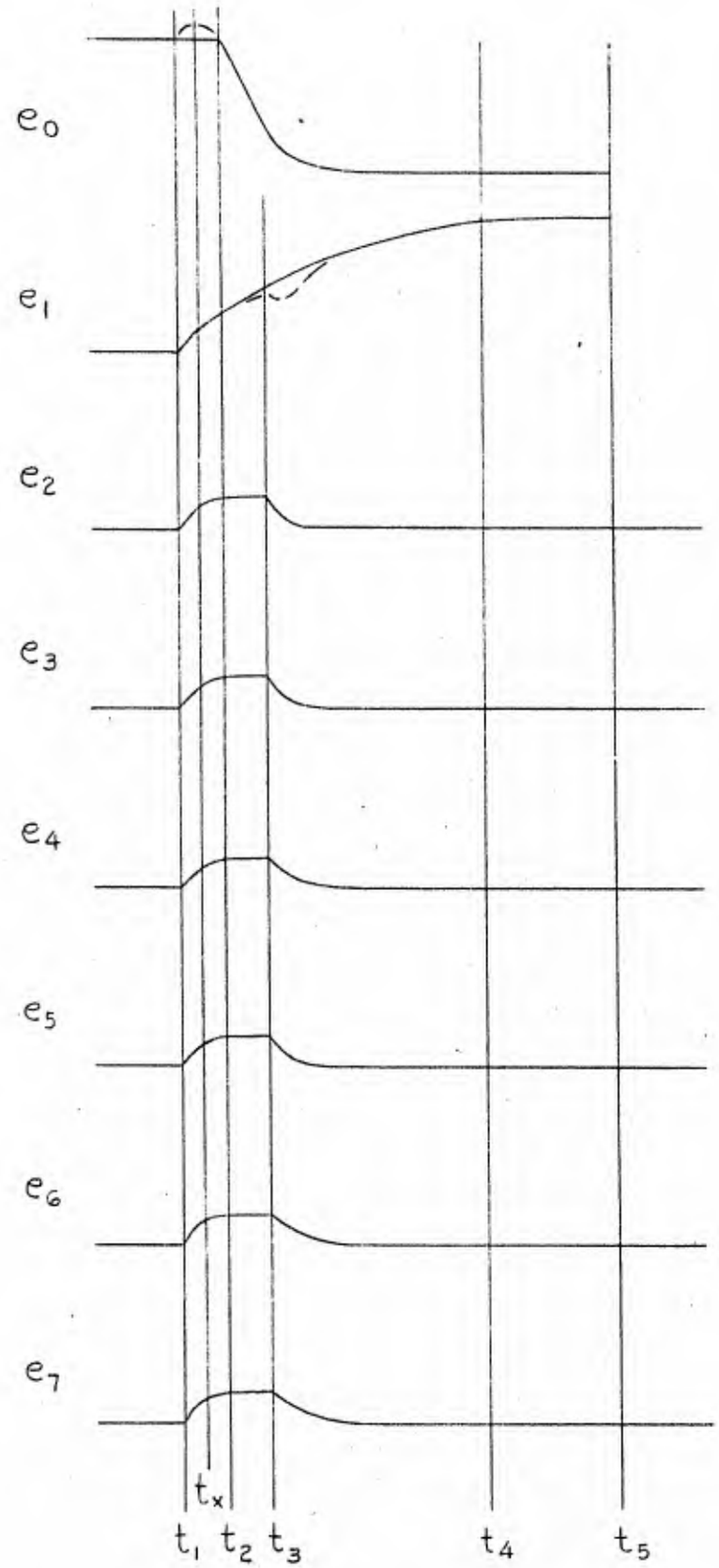


CIRCUIT DIAGRAM OF THE EIGHT-POSITION CRYSTAL-MATRIX SWITCH

USED IN D.R.B. THESIS

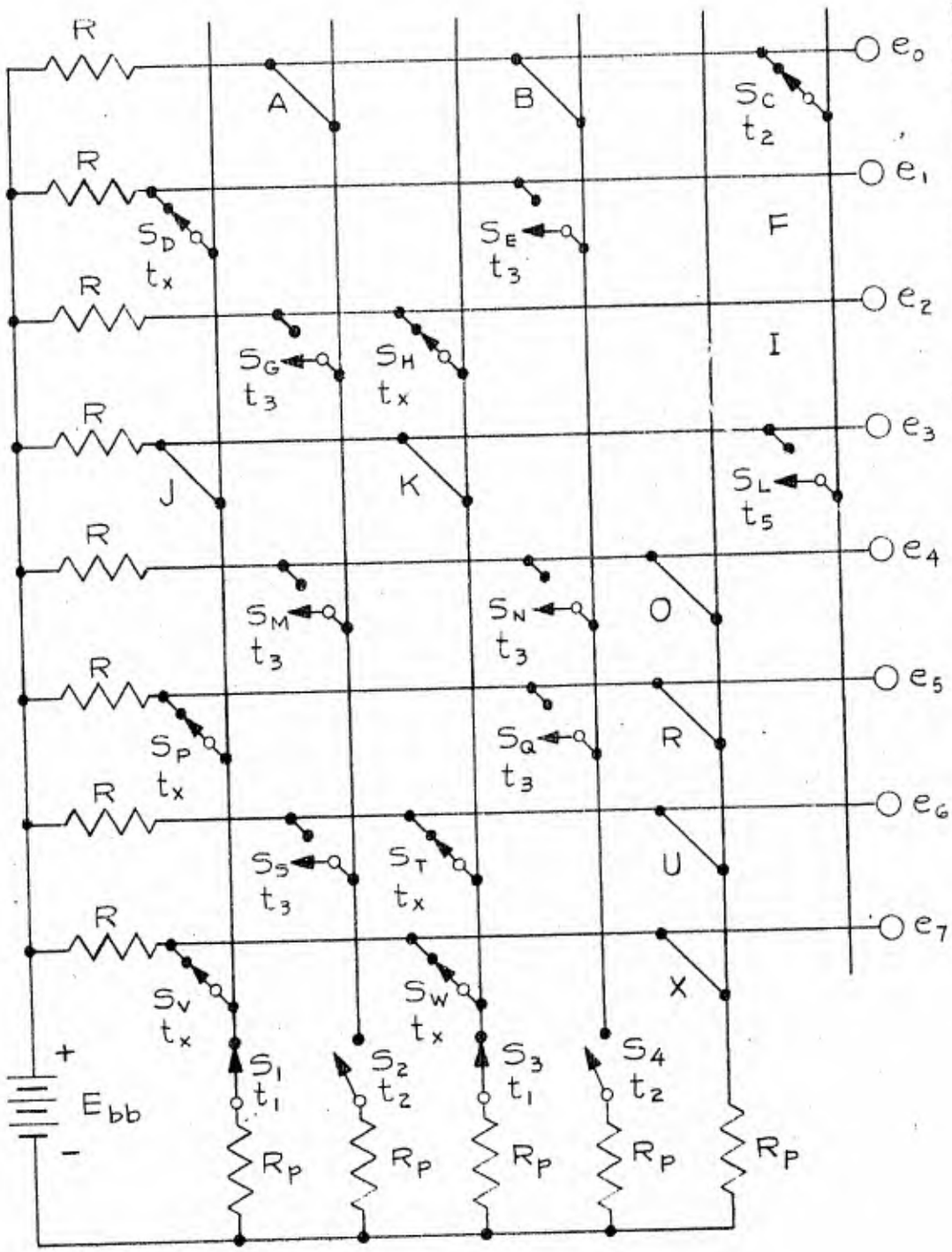


EQUIVALENT CIRCUIT OF THE EIGHT-POSITION SWITCH FOR A TRANSITION FROM TERMINAL 0 TO TERMINAL 1

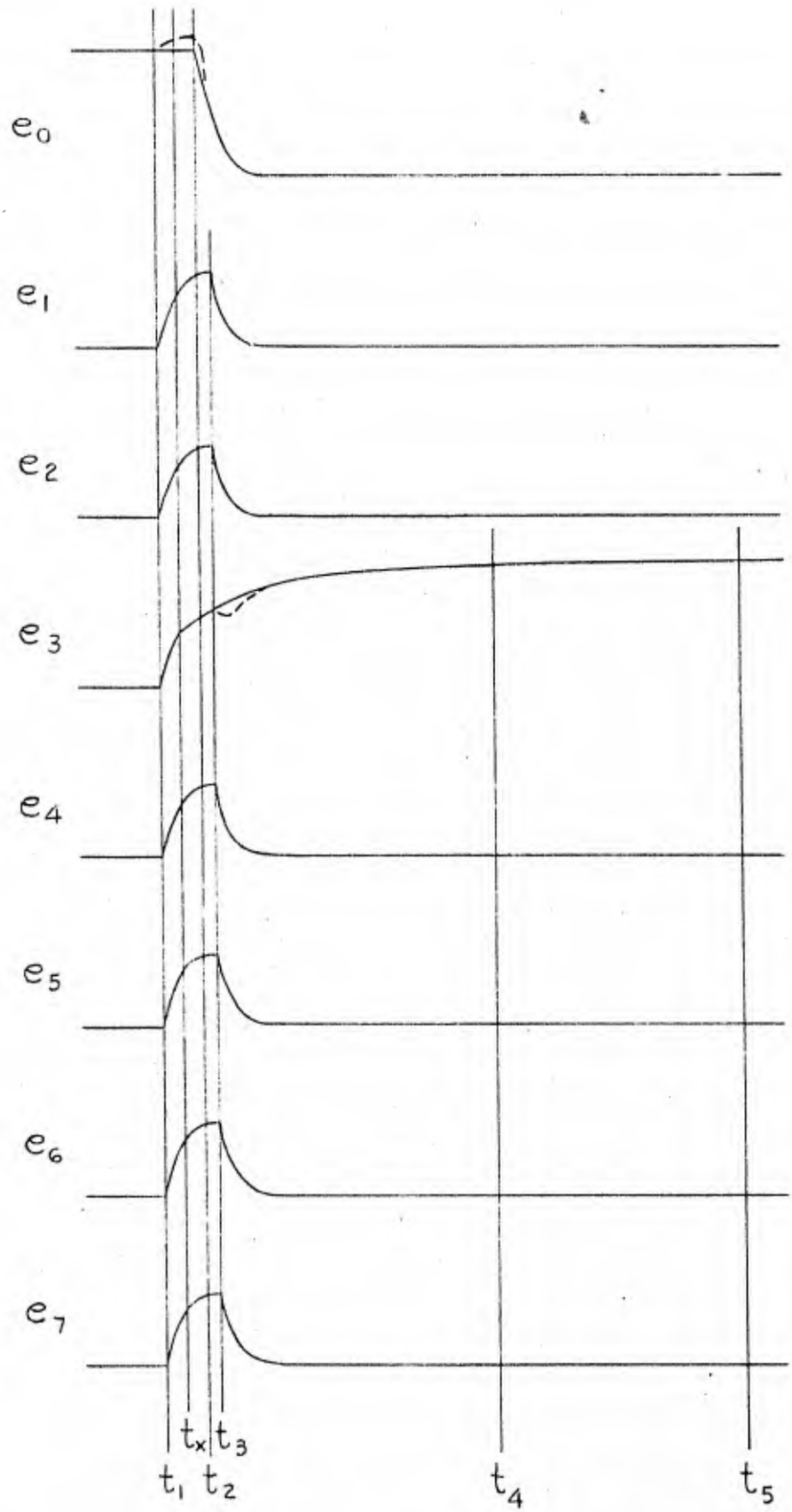


WAVEFORMS AT TERMINALS OF EIGHT-POSITION SWITCH DURING A TRANSITION FROM TERMINAL 0 TO TERMINAL 1

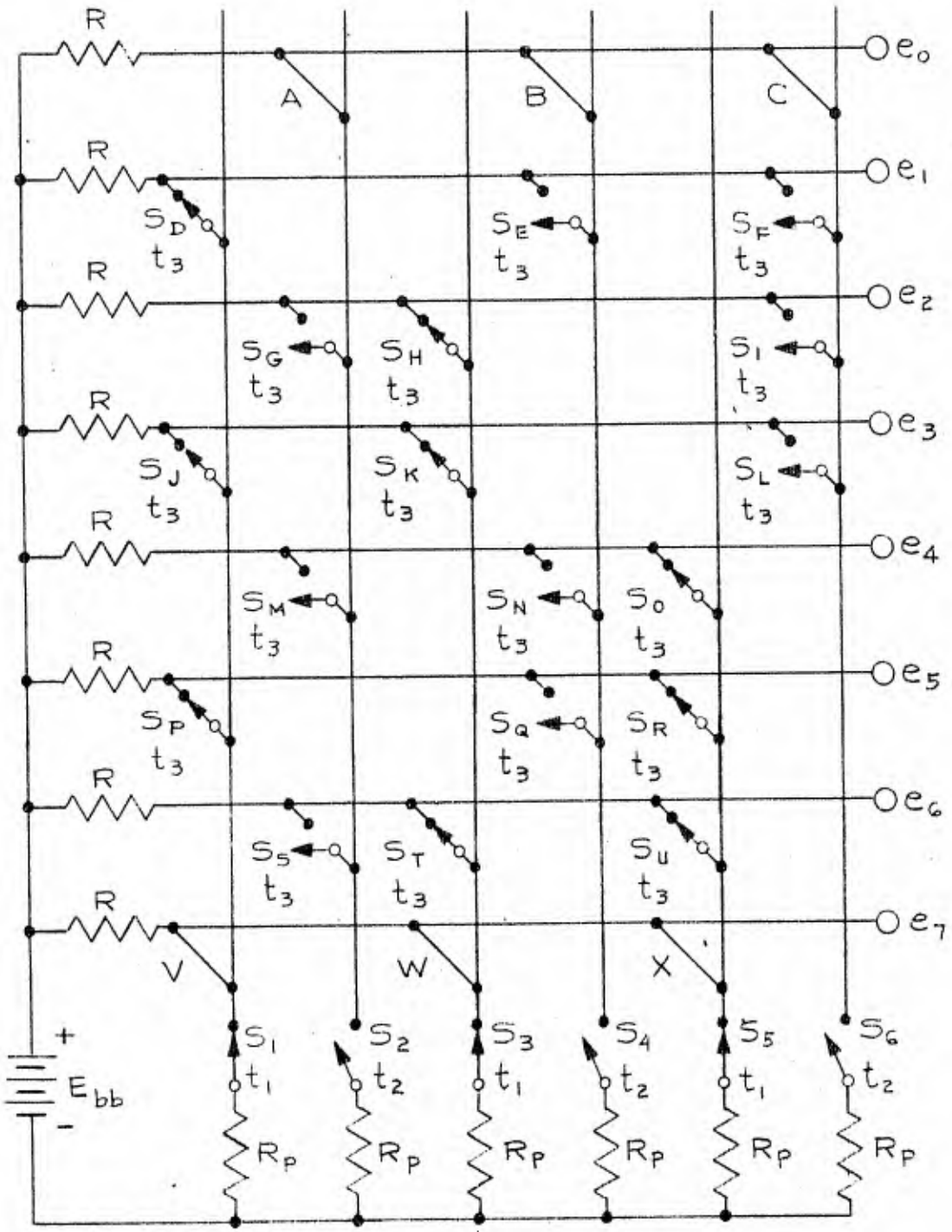
A-30542



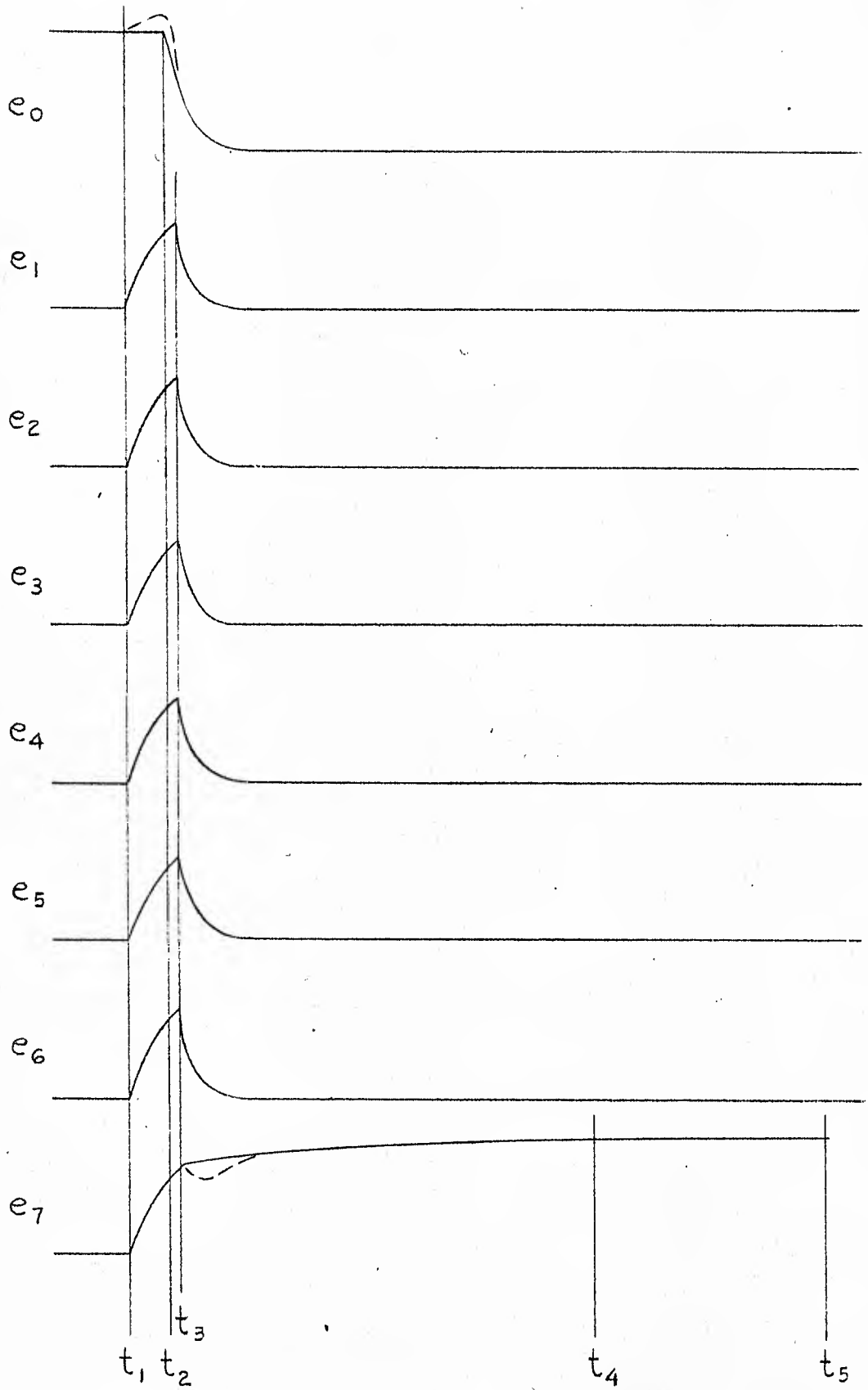
EQUIVALENT CIRCUIT OF THE EIGHT-POSITION SWITCH FOR A TRANSITION FROM TERMINAL 0 TO TERMINAL 3



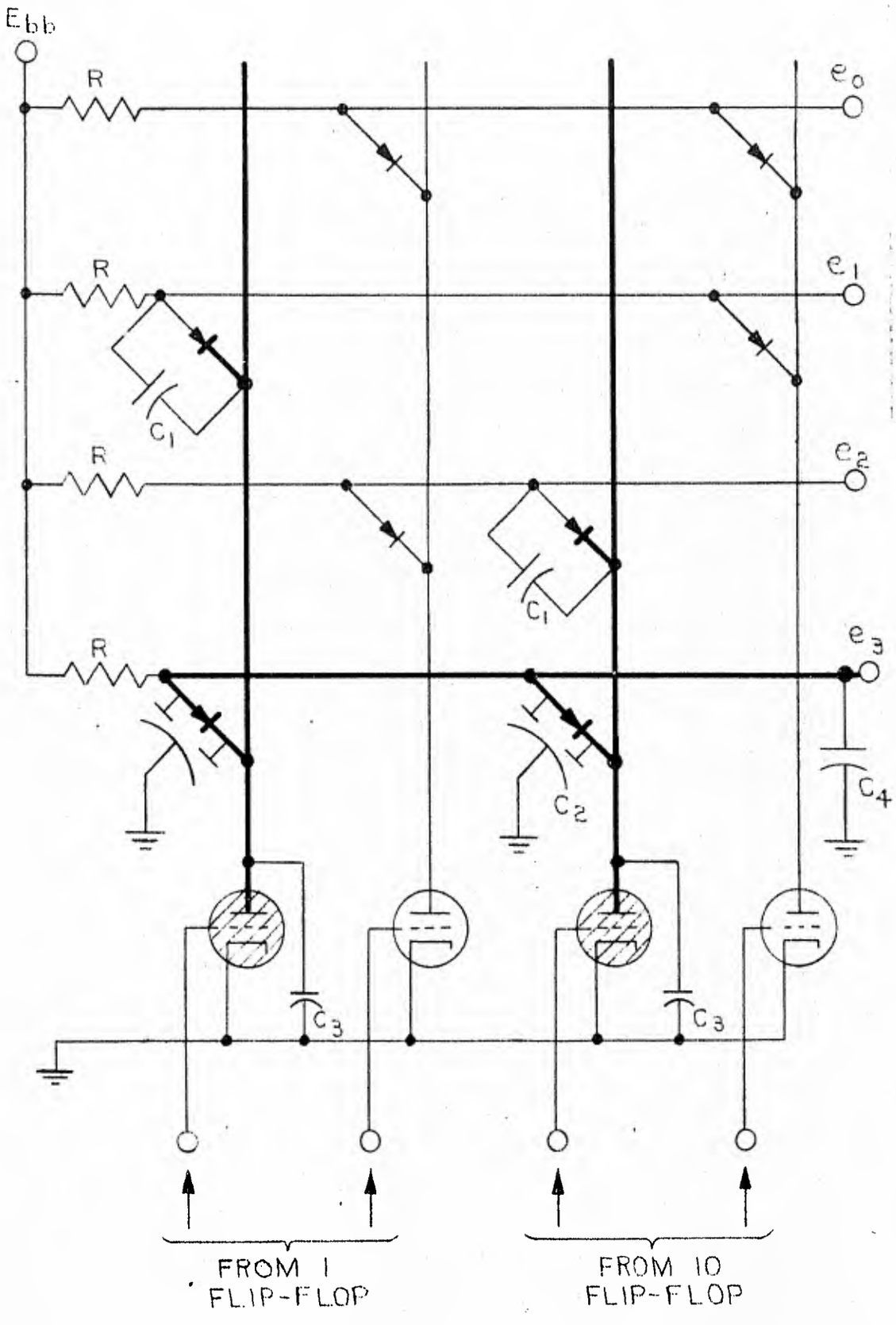
WAVEFORMS AT TERMINALS OF EIGHT-POSITION SWITCH DURING A TRANSITION FROM TERMINAL 0 TO TERMINAL 3



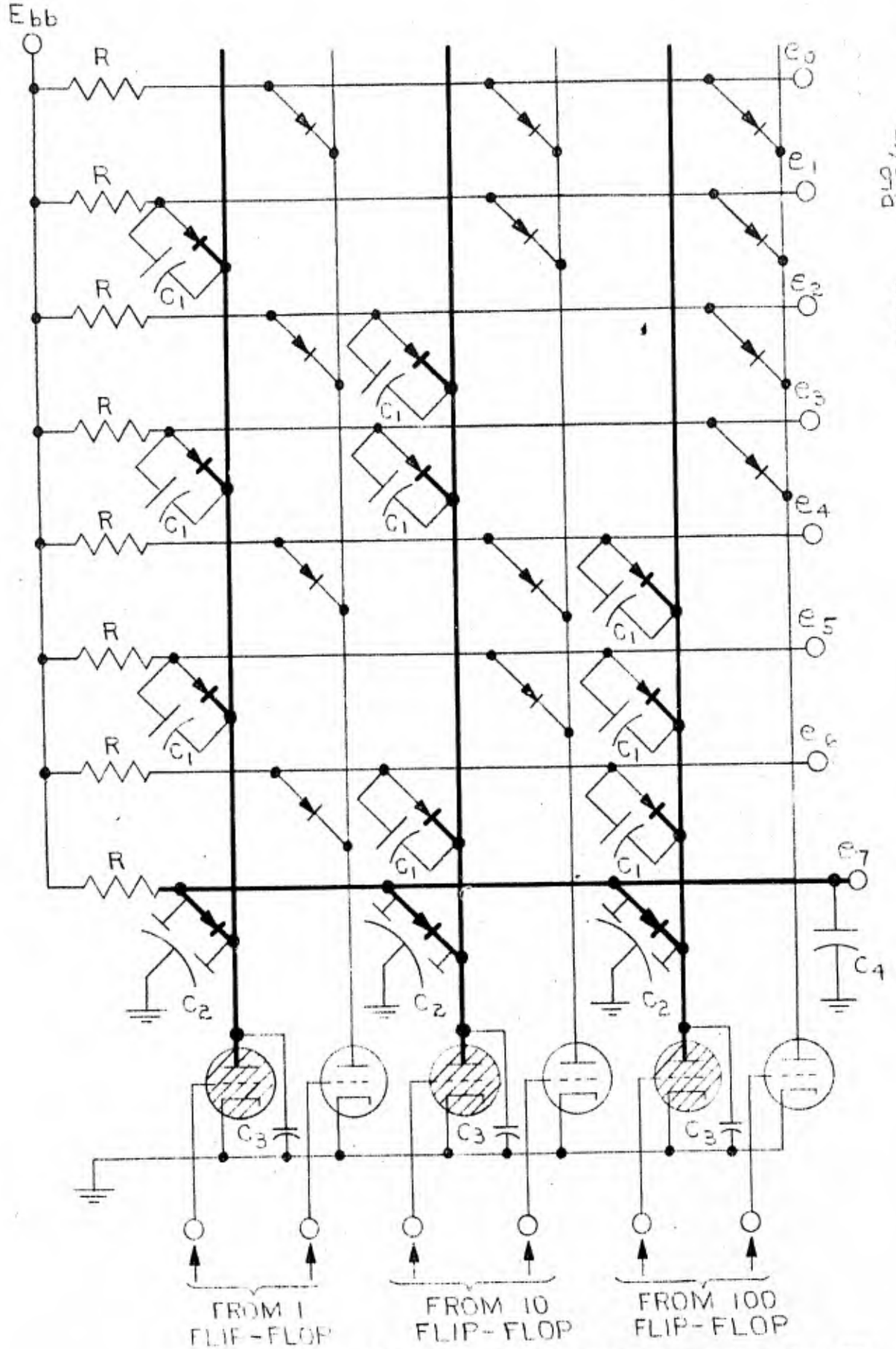
EQUIVALENT CIRCUIT OF THE EIGHT-POSITION SWITCH FOR A TRANSITION FROM TERMINAL 0 TO TERMINAL 7



WAVEFORMS AT TERMINALS OF EIGHT-POSITION SWITCH DURING A TRANSITION FROM TERMINAL 0 TO TERMINAL 7



CIRCUIT DIAGRAM OF THE FOUR-POSITION SWITCH
SHOWING THE SHUNT CAPACITIES



CIRCUIT DIAGRAM OF THE EIGHT-POSITION SWITCH SHOWING THE SHUNT CAPACITANCES

USED IN D.R.E. TYPE

6345 DLD 5/23/47 A-30543 D.R.E.

A-30548

A-38202-G

2C51/396A

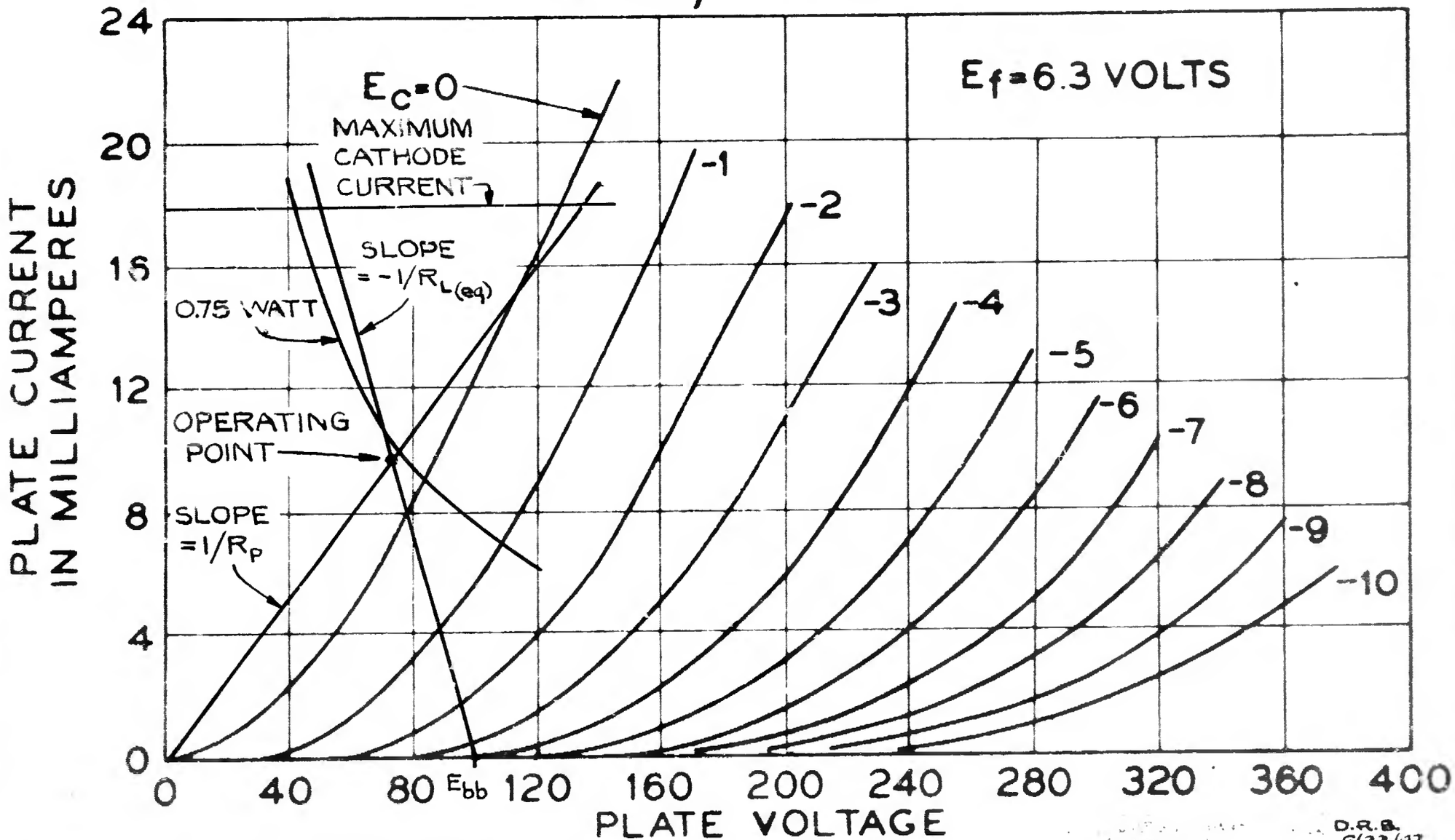


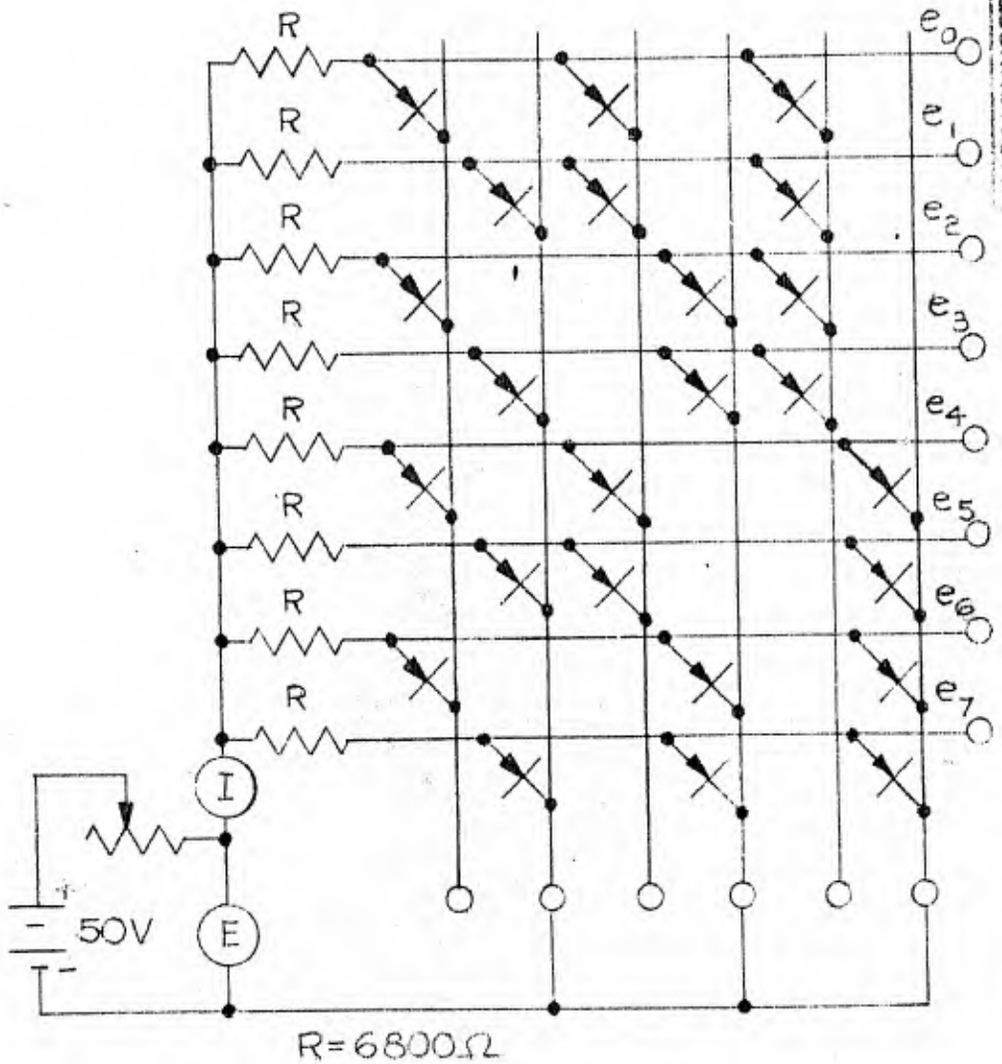
PLATE CHARACTERISTIC OF 2C51 SHOWING OPERATING POINT FOR EIGHT-POSITION SWITCH

D.R.B. 5/22/47

6345

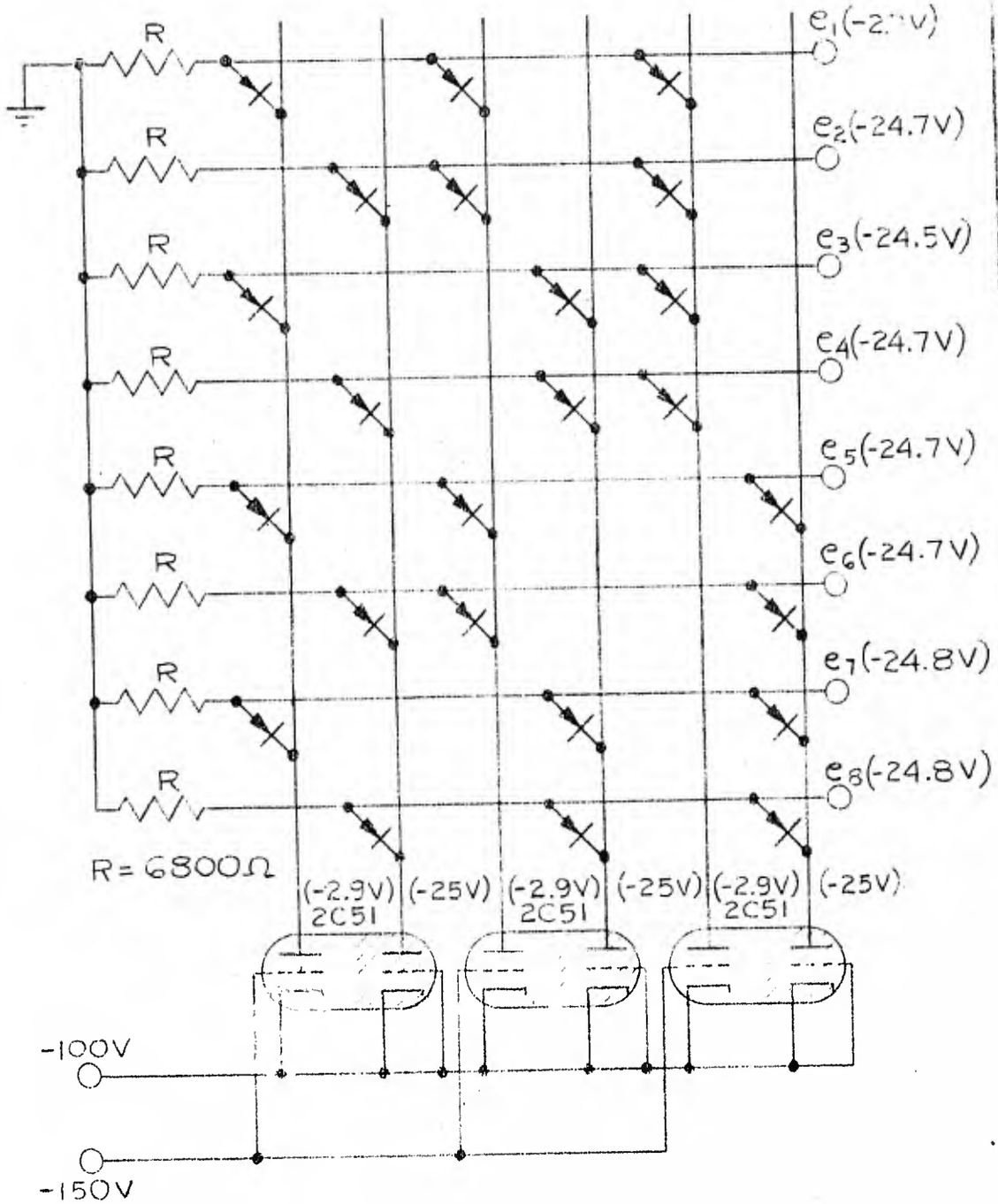
A-38202-G

USED IN D.R.B. THESIS

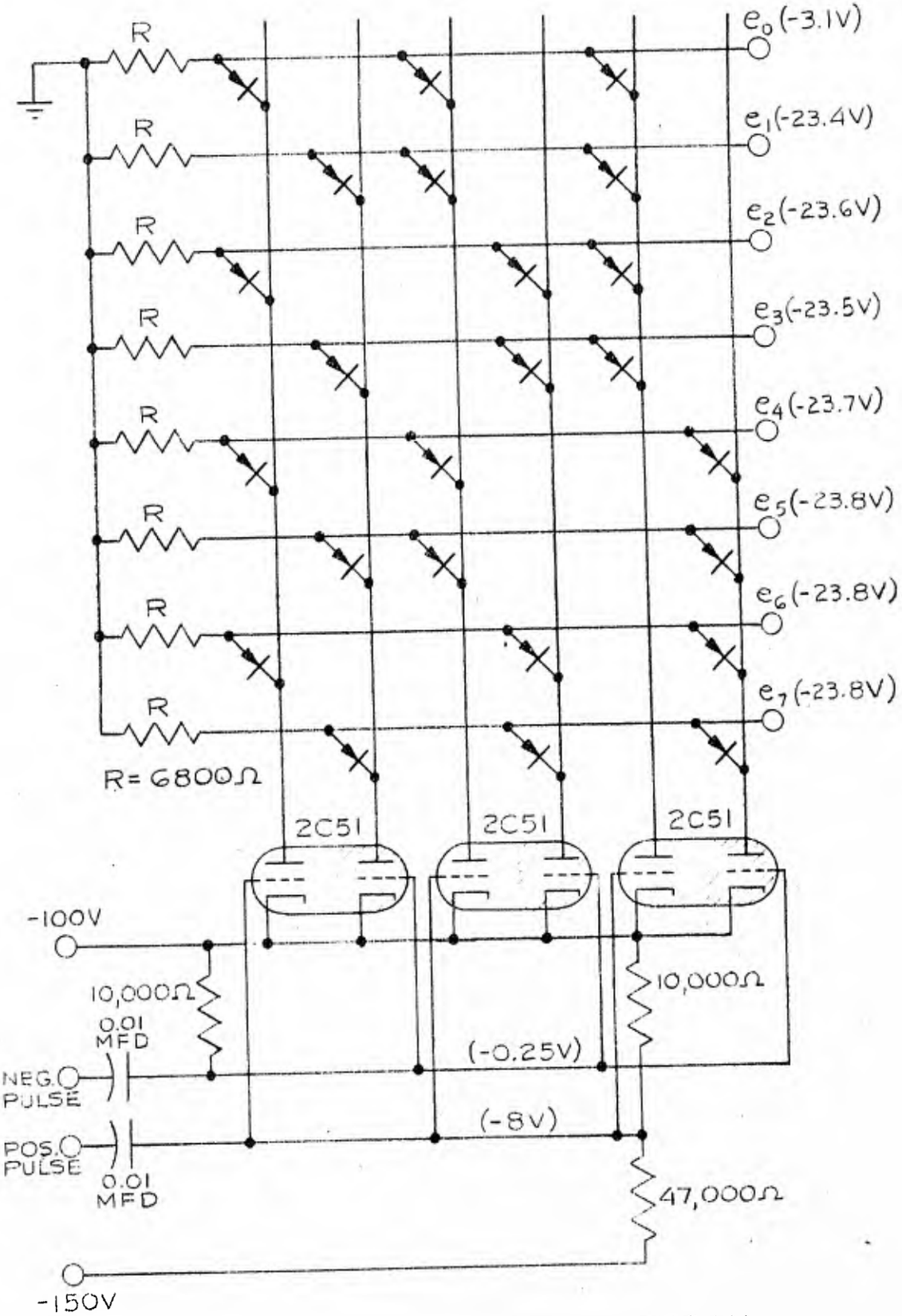


CIRCUIT FOR MEASURING $R_{L(eq)}$

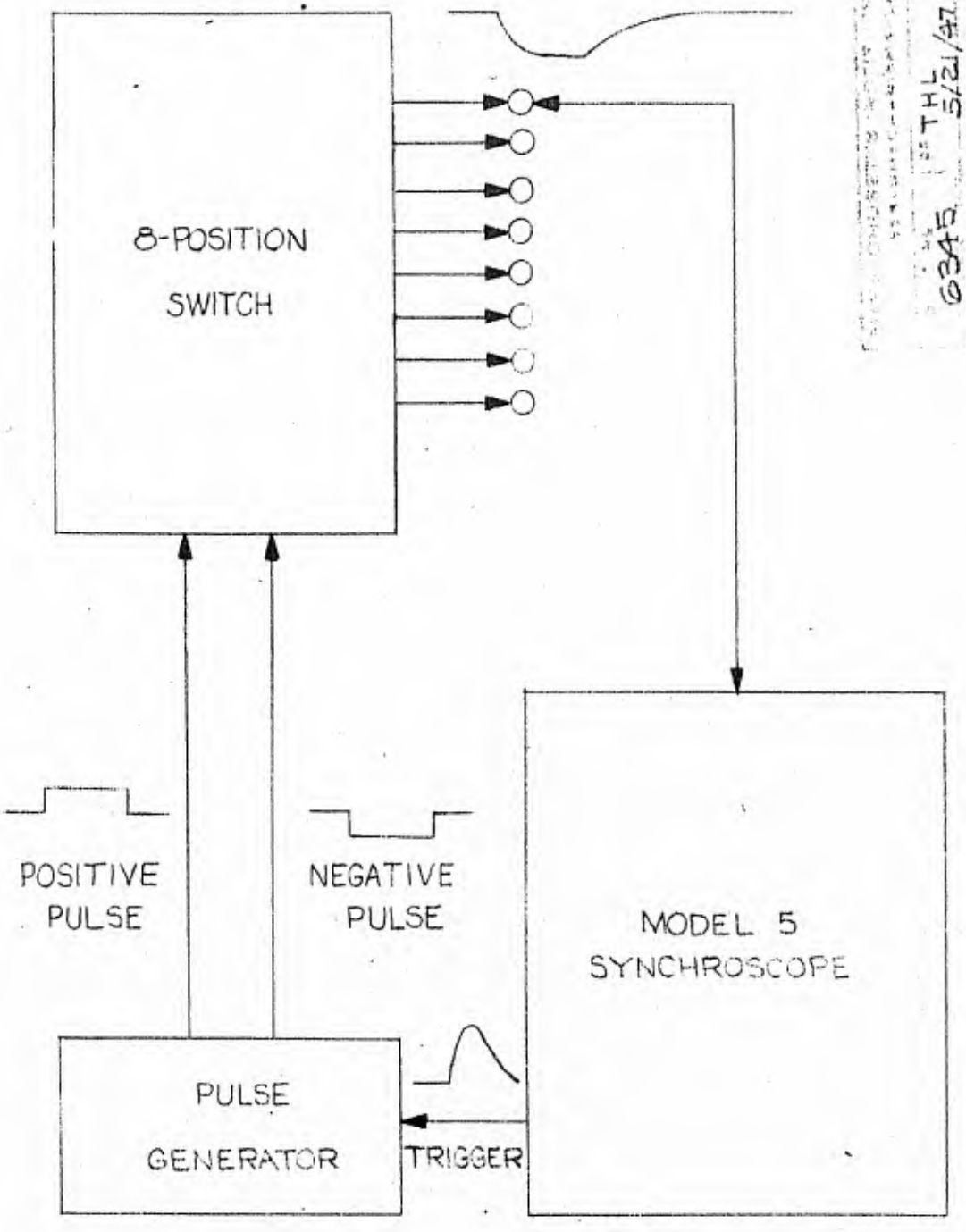
USED IN D.R.B. THESIS



CIRCUIT DIAGRAM SHOWING
CONNECTION OF BUFFER AMPLIFIERS

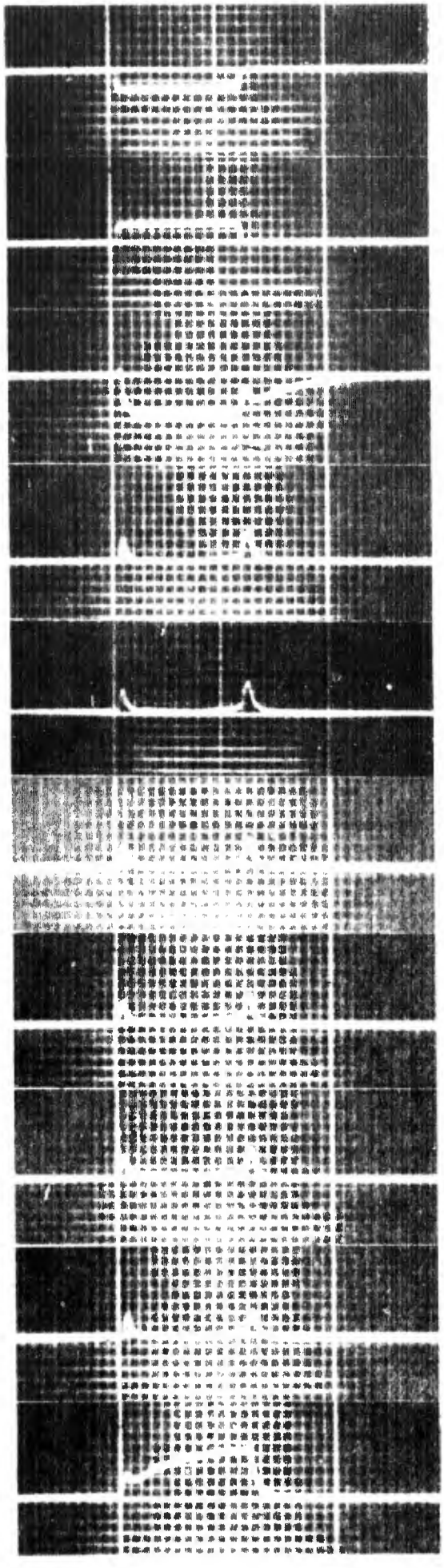


CIRCUIT USED TO CHECK
THE DYNAMIC ANALYSIS



BLOCK SCHEMATIC FOR CHECKING
THE DYNAMIC ANALYSIS

USED IN D.R.B. THESIS



NEGATIVE PULSE

POSITIVE PULSE

e_0

e_1

e_2

e_3

e_4

e_5

e_6

e_7

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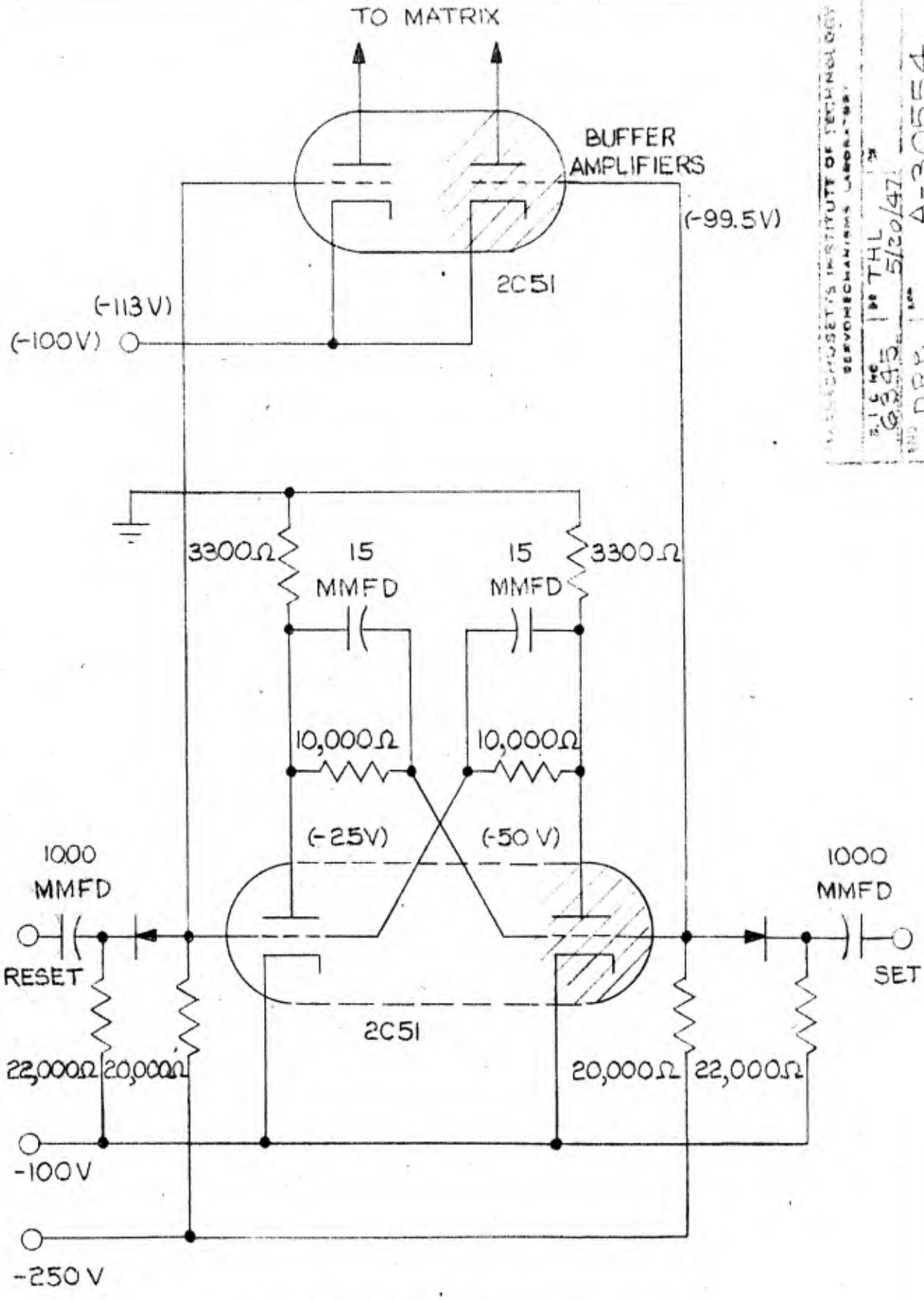
ENG. D. R. B.	APP.	A-30553	

A-30553

WAVEFORMS OBTAINED TO CHECK THE DYNAMIC ANALYSIS

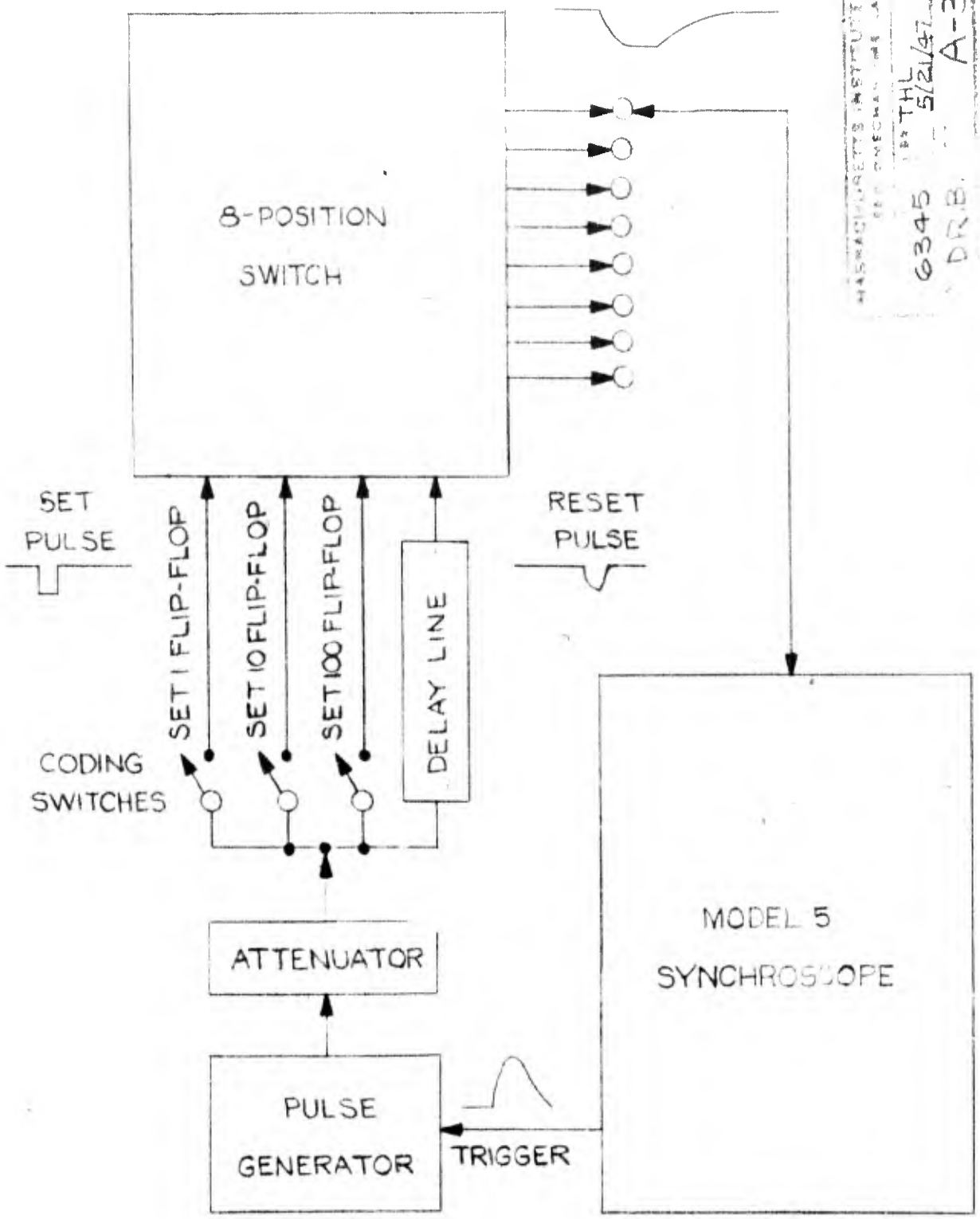
USED IN D.R.B. THESIS



CIRCUIT DIAGRAM OF FLIP-FLOP
USED WITH EIGHT-POSITION SWITCH

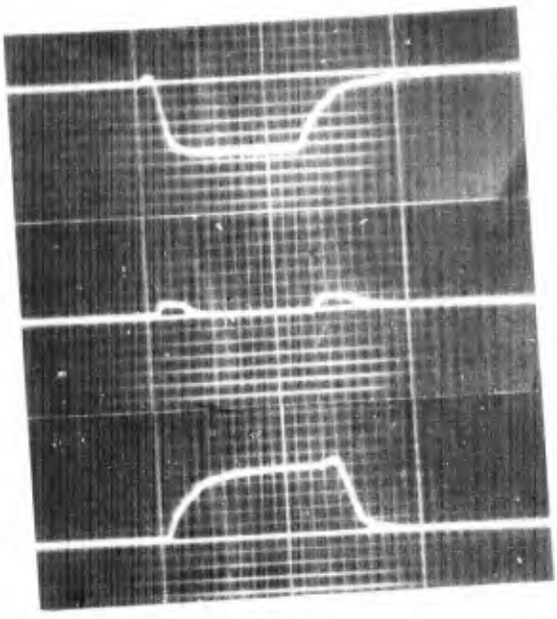
USED IN D.R.B. THESIS

A-30554



BLOCK SCHEMATIC FOR TESTING
THE EIGHT-POSITION SWITCH

USED IN D.R.B. THESIS

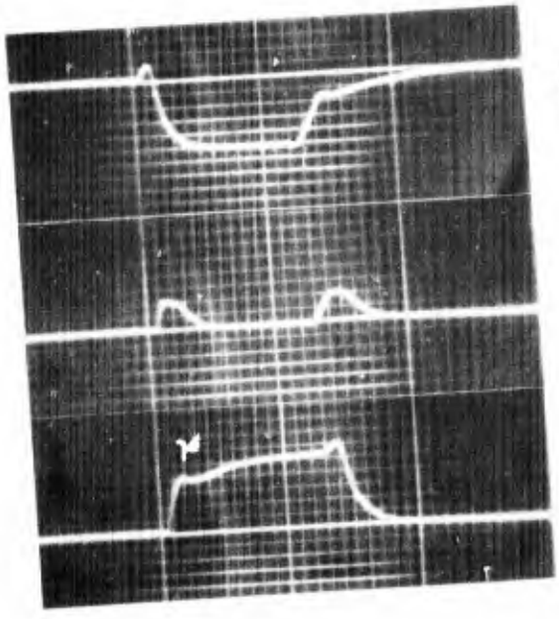


e_0

e_2

e_1

TRANSITION FROM TERMINAL 0 TO TERMINAL 1

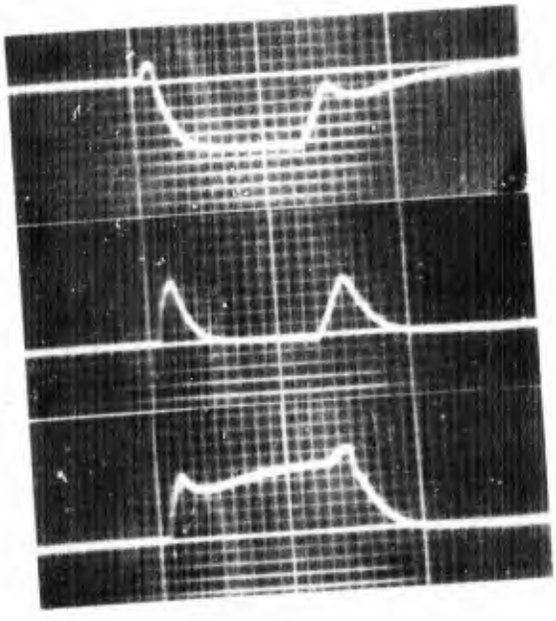


e_0

e_1

e_3

TRANSITION FROM TERMINAL 0 TO TERMINAL 3



e_0

e_1

e_7

TRANSITION FROM TERMINAL 0 TO TERMINAL 7

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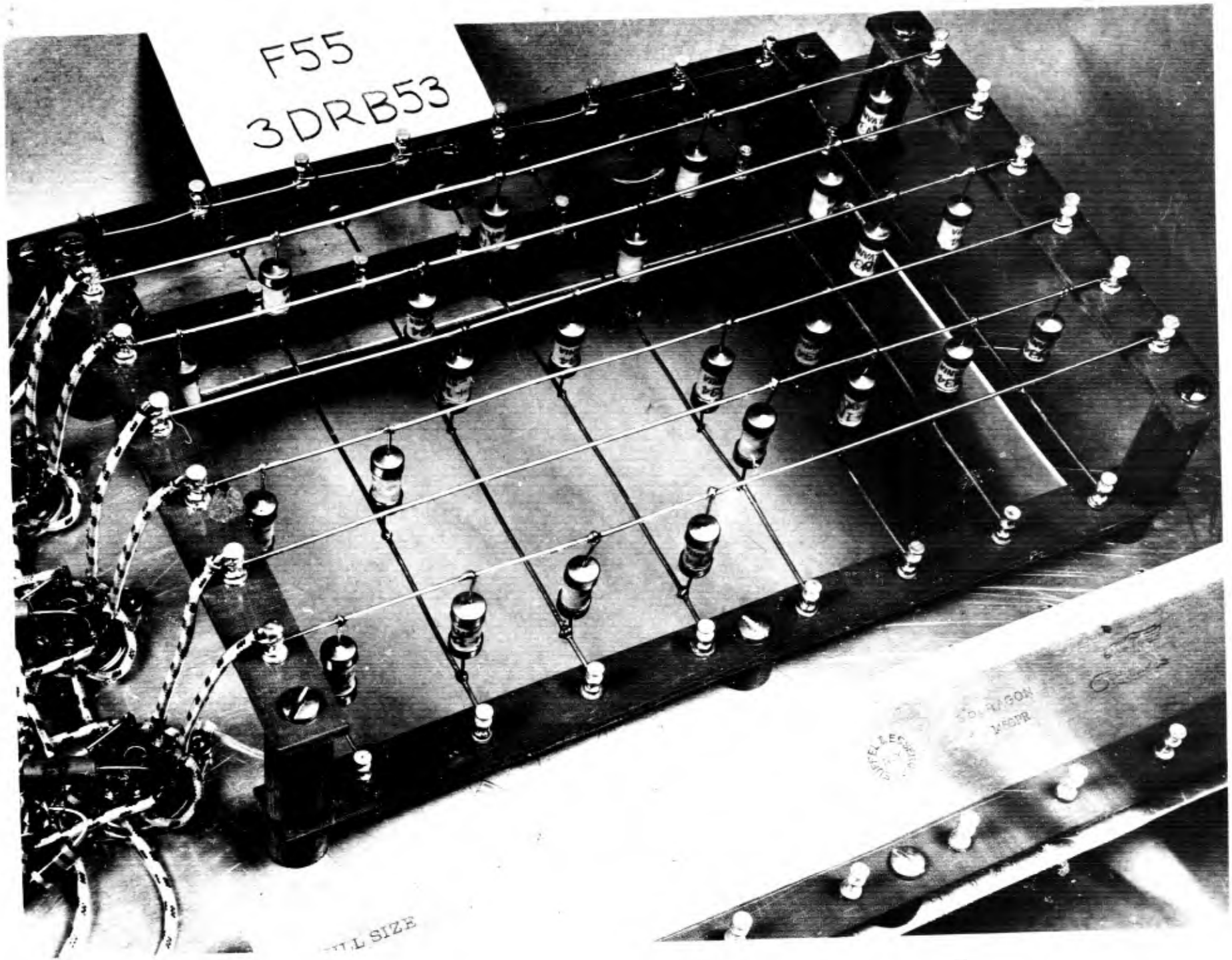
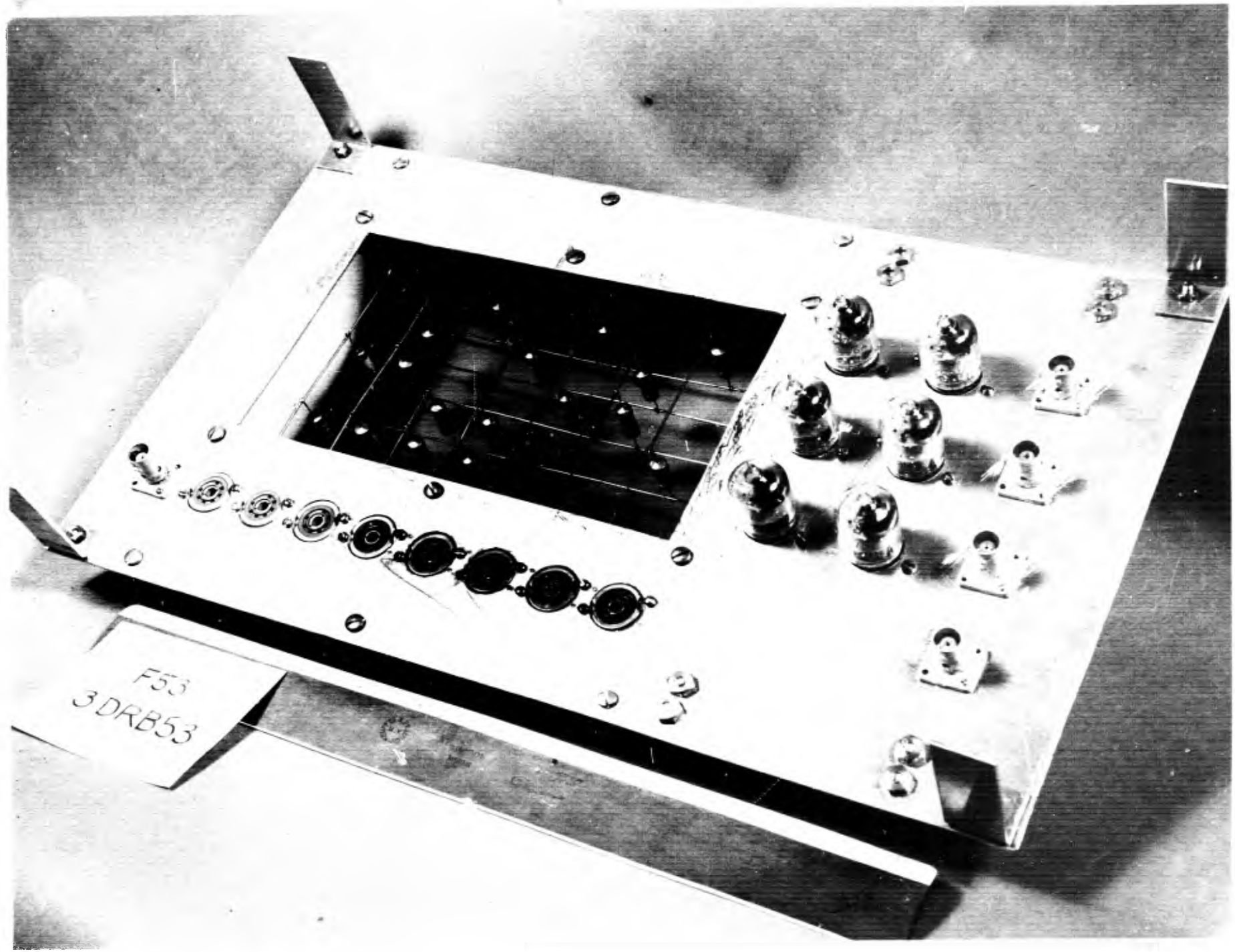
ENG. D. R. B.	APP.		

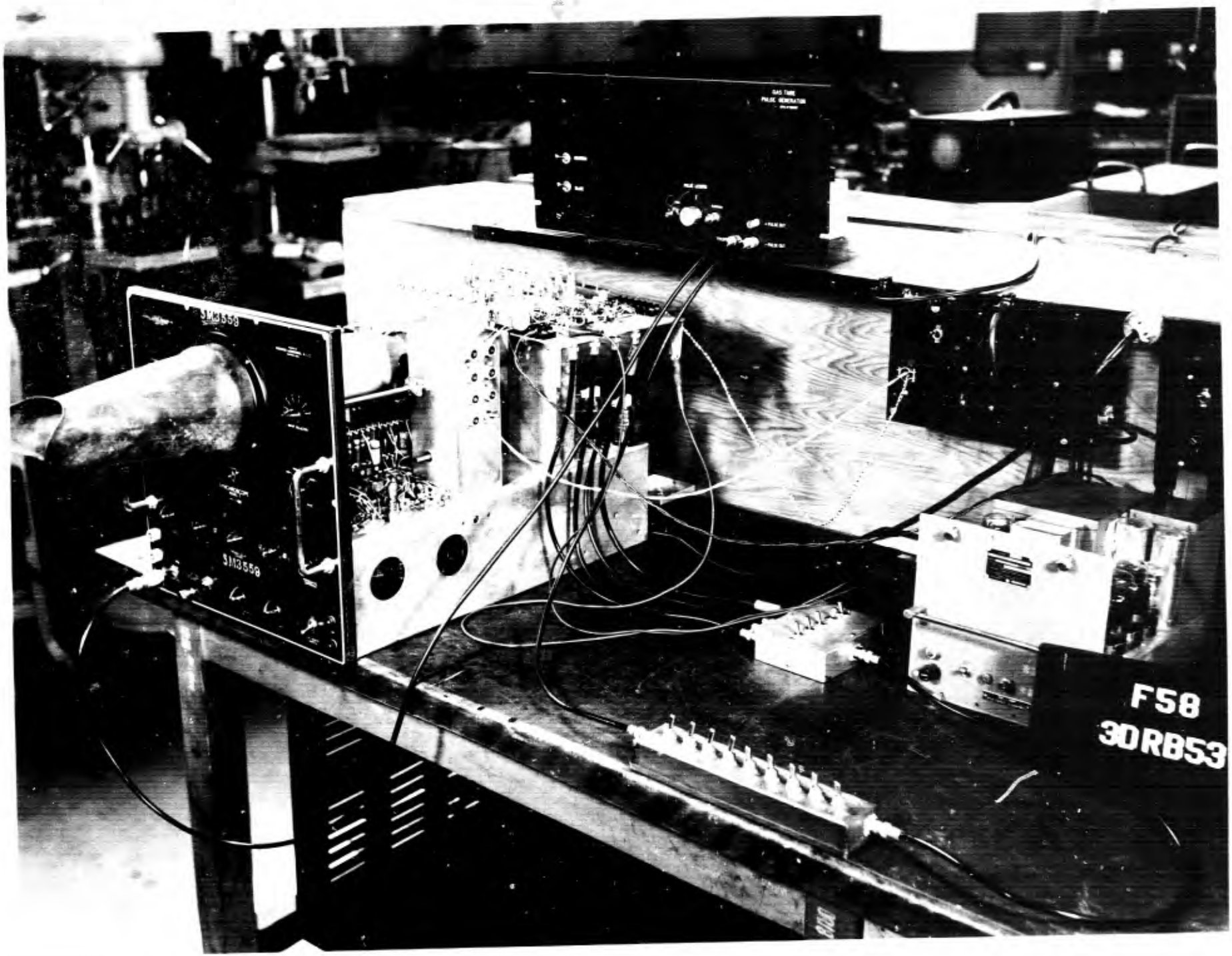
-30556

WAVEFORMS OF FIGHT—POSITION SWITCH


F55
3DRB53

F5 6
3DRB53


F53
3DRB53


F58
3DRB53

6345
Report No. R-123

SERVOMECHANISM LABORATORY
Massachusetts Institute of Technology
Cambridge, Massachusetts

Date of Report: July 15, 1947 — Page 1 of 14 pages

Subject: The Thirty-Two Position Switch — Drawings: (See List of Drawings in the Appendix)

Written by: John A. O'Brien

Reference: A High-Speed Multi-Position Electronic Switch, David R. Brown, S. M. Thesis, M.I.T., Course VI, May, 1947.

Characteristics of Sylvania 1N34 Germanium Crystal Diodes, Ray E. Ellis, 6345 Report No. R-106, December 3, 1946.

Introduction

This paper reports development of a thirty-two position electronic switch. A complete switch has been built and tested in the Laboratory; and, although the design of the switch has not reached perfection, the switch operates somewhat better than had been anticipated, being able to switch to a selected line in slightly less than 0.2 microsecond.

A five-digit binary number, represented by pulses on five input lines, determines the output line selection. Each of these pulses is used to set a flip-flop. The ten outputs of the five flip-flops are applied, through driver tubes to a matrix made up of ten vertical and thrity-two horizontal lines connected at proper cross points by germanium crystal rectifiers. The crystals are so connected that for any setting of the flip-flops only one of the thirty-two lines has no voltage on it. There are thirty-two possible combinations of the five input pulses; thus, the switch can be used to select any one of the thirty-two output lines.

Original Design

The original design of the thirty-two position switch was developed by D. R. Brown. (See Reference). That design required that transmitting-type tubes, such as the 825 or 3329, be used to drive the crystal matrix, and that 1200-ohm load resistors

be used to terminate the matrix output lines. Extrapolating from the work done on an eight-position switch, the switching time of the thirty-two position switch was estimated to be one-half microsecond. Drawing D-30672 shows the simplified circuit schematic of the final 32-position switch. This circuit is similar to the original design with the exception of the 7F8 cathode followers.

Physical Considerations

It was decided that the switch be constructed to mount on a standard relay rack. This would facilitate testing and be more in line with the probable final design. The vertical panel arrangement would also make for better cooling of the tubes by convection. A rear view of the switch rack is shown in Drawing A-30696.

As can be seen from the photographs, Drawings A-30694 and A-30695, the crystal matrix is mounted in a rigid framework of one-half inch laminated phenolic. This was done to provide a demountable rigid unit to facilitate placement and testing of the crystals. The dimensions of the matrix were determined by the size of the panel and the size of the input and output tube sockets. The stray capacitance between the wires of the matrix was also considered, and estimates using the results of the eight-position switch indicated that a matrix large enough to satisfy the tube spacing would not give too much stray capacitance.

The overall dimensions of the matrix frame are fourteen inches wide by thirty-two and three-fourths inches high (32-3/4"). The wires in the matrix are bare, fifteen-gauge tinned copper. The horizontal wires are one inch apart which is just about minimum spacing that can be allowed for the tube sockets of the output amplifiers. The wires of the vertical pairs are one inch apart and the pairs are spaced two and three fourths inches (2-3/4") between centers. The circuit schematic of the final matrix is shown in Drawing A-30676.

The matrix drivers are mounted directly below the matrix on the panel, as is shown in Drawing A-30693; 5829 tubes are used for the drivers and since the plate connections of this tube come out of the top of the tube, holes were cut in the panel through which the plate leads could be connected to the matrix inputs.

Below the drivers and on a separate panel, the switching flip-flops were mounted. These are shown in Drawing A-30695.

In the type of construction used, wherever possible, wiring appears on the front of the panel where it is easily accessible.

Static Measurements of Matrix

Before inserting the crystals in the matrix, capacitance measurements were made, with input wires connected to 5829 plates and output wires connected to tubeless sockets. Capacity measured was that between one wire and ground with all other wires grounded. The capacitance of a vertical wire is twenty-four micromicrofarads and of a horizontal wire, nine micromicrofarads. From these tests, it was found that the input wires should have about half an inch of clearance where they pass through the panel. These capacitances are somewhat higher than had been estimated, but they could be reduced by using smaller wire, and cutting out the portion of the panel behind the matrix.

Proper operation of the crystal matrix is dependent upon the forward and back resistances of the crystals used. The design of the matrix specified a forward resistance of less than 100 ohms and a back resistance of more than 100,000 ohms. In order to maintain these specifications, all crystals were tested and only those surpassing the specifications were used. Sylvania type 1N34 crystals were used, and the details of the characteristics of these crystals are given in the reference report, R-106.

After the crystals had been inserted in the matrix, static tests were made on the matrix to determine the potential differences to be expected between selected and unselected lines and to find any crystals that might be bad. These tests were made by terminating the output lines with 1200 ohms to ground and then applying a common negative voltage to one side of each pair of input lines. In this test, various voltages were used, but the voltage expected in the final switch was to be about 23 volts, so most of the tests were run using a 24-volt storage battery source. Drawing A-30678 shows the matrix connections used in this test. By applying a -24.3 volt supply voltage to different sides of the input pairs, the selected terminal was found to have a voltage of about -3.8 volts and the unselected terminal had a voltage of about -23.5 volts. This varied from -23.0 volts at terminal No. 2 to -23.9 volts at terminal No. 32.

If the crystals in the matrix had an infinite back

resistance, then the voltage on the selected terminal would be zero. The finite back resistance of the crystals allows some current to flow from the selected output line to the unenergized input lines and then through the back resistance of the crystals connected to the unselected output lines; thus some voltage appears on the selected outputs. If any one of the crystals in the matrix has a low back resistance, then any output line connected through crystals to the same input line as the bad crystal will have a voltage larger than minus four volts appearing on it when selected. There are sixteen crystals connected to each input line; thus the bad crystal will cause an incorrect selected voltage on fifteen lines. When the fifteen incorrect outputs are found, inspection of the matrix schematic will show the bad crystal.

In the case observed, lines No. 18 to No. 32 showed a selected voltage of -5.5 volts whereas all others were -3.8 volts. This indicated a bad crystal between output No. 17 and one side of the No. 5 input pair.

In the case of an open-circuit crystal, the line to which it is connected will appear as a selected line when it should not. The open-circuit crystal is the one connected to that input line which is not connected through crystals to both the true selected output and the false selected output.

Matrix Drivers

Following these tests, the 5E29 tubes were wired to drive the matrix, and an attempt was made to test the system by allowing one-half of each tube to conduct and biasing off the other half. However, no selected line indications could be found and it was discovered that the system was oscillating. The oscillations were prevented by inserting a 100-ohm resistor in each control-grid lead of the 5E29's. With the cathodes of the drivers connected to a supply of -150 volts, one side of each driver biased to cutoff and the other side at zero bias, the voltage on a selected line was measured at minus four volts and the unselected lines measured between minus twenty-three and minus twenty-four volts. These measurements confirmed the original estimates of the operating points.

The driver tubes operate with a plate to cathode and a screen to cathode voltage of 150 volts. When the tube is conducting with zero bias, the plate current is approximately 120 ma, with a plate voltage of 125 volts, and the screen current is about 13 ma.

Under these conditions the plate dissipation is 15 watts and the screen dissipation is 2.7 watts. The manufacturers do not give the natural-air-cooled dissipation ratings for continuous operation of this tube, but the intermittent operation ratings are 40 watts and 6 watts for plate and screen dissipations respectively for the two sections of the tube together. In the electronic switch, only one section of the tube operates at one time, and it would seem that the 15 watts and 3.7 watts are not excessive. The effective plate load of the driver tubes is 200 ohms, and the "cutoff" bias required is about 30 volts.

Tests were then made using positive and negative pulses to determine the switching time of the matrix. Positive pulses were applied to the grids of the "off" drivers, and negative pulses were applied to the grids of the "on" drivers. The results of these tests showed a switching time of well over one microsecond, but the shape of the pulses available for this test was poor; so little weight was given to these results. Since at this point the construction of the switching flip-flops was very nearly completed, the pulse tests were dropped, and attention turned to completing the flip-flops.

Switching Flip-Flops

The circuit schematic for the switching flip-flops is shown in Drawing A-39237-3. This flip-flop is essentially the same as the standard circuit except that the triggering tube is biased below cutoff by a portion of the voltage across the cathode resistor of the flip-flops. The voltage appearing between cathode and ground is about thirty-two volts and eleven volts of this is used to bias the triggering tube. This bias insures against small triggers reversing the flip-flop. The plate signal swing of the flip-flop is about twenty-seven volts.

In the setup used, the sockets for all five of the flip-flops were mounted on one panel and the filaments and ground leads connected. The components for the individual flip-flops were mounted on separate special terminal boards and then bolted down over the tube sockets and connected. This method was used to facilitate replacement of the flip-flops, but it requires about an hour to change one, so the method is not recommended. It might be better to mount the tube sockets on the component panel and thus only seven connections would have to be broken and remade for a replacement. These are supply voltage, ground, set, reset, restorer, and the two output leads.

The flip-flops were constructed and tests were run on them to observe the restoring operation. In the restoring operation, the flip-flop is triggered twice in quick succession (one microsecond) thus causing it to reverse itself and then return, or to flip to its other position and return. The purpose of the restoring operation is to allow a-c coupling from the flip-flops to succeeding stages. At the plates of the flip-flop a pulse appears whose length approximates the length of the restoring interval. The polarity of this pulse depends upon which position the flip-flop was in before the triggers arrived. These pulses can be transmitted through an a-c coupling circuit to a clamping circuit. During this test the flip-flops were found to be somewhat unsatisfactory in that, in spite of their supposedly identical construction, one of the flip-flops tended to oscillate and was not very stable. This was found to be caused by a very slight unbalance in grid return resistors and was aggravated by unmatched tubes. This difficulty was corrected by "tailoring" the individual flip-flops.

It is desired that any flip-flops used in a circuit of this type be of such design that any flip-flop constructed of standard parts, will operate in the same manner as all others based on the same design. The fact that any flip-flop must be individually adjusted indicates that the design is somewhat unstable. A new flip-flop has been designed since, and given Drawing No. SB-39272-S not shown in this report. Tests on the new flip-flop are not complete.

A-C Coupling

The flip-flops are a-c coupled to the drivers through a clamping circuit, Drawing A-30667. The clamping circuit consists of a 780-micromicrofarad coupling condenser from the flip-flop plate to the driver grid, and a 1N34 crystal from driver grid to cathode. The circuit is connected to clamp on the positive side of the driver grid waveform, thus the grid receiving a positive pulse during the restoration is "cutoff" for the rest of the cycle, and the other side of that driver, receiving negative pulses, is conducting during the rest of the cycle. Assuming the flip-flop to be in the "zero" or "cleared" position, then a "set" pulse will invert the output waveforms of the flip-flop and thus reverse the operation of the corresponding driver tube; this constitutes a switching operation. A reset pulse applied to the flip-flops will return the system to its original condition. The value of 100 micromicrofarads originally used in the coupling circuit was found to be too small to hold the driver cut off for the full ten-

microsecond complement period. A 680 micromicrofarad capacitor was added to the coupling circuit and this provided satisfactory operation. This gave a total value of 780 micromicrofarads in the coupling circuit.

Operation Tests

The block schematic of the test setup used in testing the complete switch is shown in Drawing E-30677-1. In the first tests no toggle-switch storage was used and the followers in the driver circuits had not been developed. The method used in testing the switch was as follows: A one megacycle clock was used to generate pulses at a P.R.F. of one megacycle; these were divided to 100 k.c. by a decade counter. From the decade counter the pulses were sent through a shaper-and-peaker circuit, Drawing A-30457, which put out 0.35 microsecond positive pulses which were inverted by a pulse transformer. These were fed into a restorer pulse generator, Drawing A-30247-2, which produced two positive pulses, one microsecond apart, from each input pulse. These double pulses were then applied to the restorer terminals of the switching flip-flops. Thus, the restoring operation took place once every ten microseconds.

The output of the first decade counter was also applied to the input of a second decade counter whose output was a positive pulse with a P.R.F. of 10 k.c. These pulses were applied to the inputs of two gate-and-delayed-trigger generators which produced positive gates of variable width. The gate pulses were differentiated and clipped, Drawing A-30674, to obtain negative pulses occurring at the time of fall of the gate. By varying the width of the gates, the timing of the negative triggers can be varied with respect to the restorer pulses and with respect to one another. One of the negative pulses was applied to the reset terminals of all flip-flops and the other negative pulse was connected to a coding box containing five switches, Drawing A-30674, by means of which the pulse could be applied to any or all of the set terminals of theflip-flops. By this means, the flip-flops may be "set" once for every ten restoring operations and are always reset once in the same period. This gives a period of 1.00 microseconds to the test cycle. The output of the second counter is of the proper frequency to synchronize a synchroscope, but the additional load on that counter output is enough to cause the gate-and-delayed-trigger generators to stop operating. For this reason a third counter was used to divide the output of the first counter for use in synchronizing the Model 5

Synchroscope.

The results of the first operation tests showed that the switching time of the switch was much too slow. In the case of switching to the thirty-second terminal, the switching time was almost a full microsecond. The trouble was that a negative pulse was coupled through stray capacitance to the selected line. A terminal is selected by cutting "off" those tubes that draw current through the crystals connected to that line, and thereby allowing that line to rise toward ground potential by discharging its distributed capacitance. Also, at almost the same time, an equal number of tubes in the driver stage are turned "on", pulling down the voltage on all unselected lines. This voltage drop is capacitively coupled to the selected line so that shortly after it has begun to rise it is drawn down and then must rise in voltage again. In the case of switching to the thirty-second position, the maximum number of input lines change voltage with a consequently greater effect of stray capacity coupling and the voltage drop coupled to the thirty-second line is enough to bring the voltage down below that of an unselected line before it rises to its final selected level.

The first attempt at improving the rise time was by means of inductances in series with the output load resistors. Both 200-and 600-microhenry chokes were tried on one line, and it was found that they helped a little, but when 200-microhenry chokes were connected to all of the lines, very bad ringing was observed. Fifty-microhenry chokes were connected on all of the outputs without causing any ringing, but the decrease in switching time was very slight.

The faults in the operation of the switch made it appear that some sort of push-pull operation might be employed to overcome the effects of the capacitively coupled voltage drop, and at the same time provide a faster rise on the selected line by raising the voltage to which the selected line was rising. In the first tests the selected line only rose to a voltage of minus four volts, and it would be much better if it would rise to zero potential or ground.

The Cathode Follower

Shown in Drawing A-30667 is the schematic of the cathode follower circuit built in order to overcome the causes of the slow switching time mentioned previously.

The scheme of the unit is that it should put out a positive pulse on the lines connected to the plates of the cutoff tubes at the same time that the unwanted capacitively coupled drop

occurs. The positive signal was available in the rise of voltage on the grid of the opposite half of the 3E29. All that was needed was to differentiate and delay that rise and apply it to the grid of the cathode follower. The 7F8 tubes would operate at zero bias and therefore would draw a small amount of zero signal current. It was hoped that this current would aid in raising the final value of the selected line voltage to zero by cancelling out the stray currents flowing through the selected line load resistor.

Operation of the Complete Switch

In Figs. F-143-1 to F-143-18 of Drawings A-30668 to A-30671 are shown the waveforms taken at various points of the switch with the 7F8 cathode followers in operation, and an output load, simulating toggle-switch storage, connected to the first four output lines of the switch. The complete block diagram of the setup used in this test is shown in Drawing B-30677; a simplified schematic of the 32-position switch is shown in Drawing D-30672, the detailed schematic of the switch output amplifier and storage input amplifier are shown in Drawing A-30673, and the schematic of the dead storage toggle switch bank is shown in Drawing A-30675.

The Figs. F-143-1 to F-143-15 inclusive have a horizontal scale of 0.5 microsecond per small division and a vertical scale of 6.2 volts per small division. Figs. F-143-16 to F-143-18 have a horizontal scale of 0.1 microsecond per small division. Drawing A-30695 shows the complete 32-position switch and the test equipment.

Fig. F-143-1 shows the restorer pulses applied to the restorer terminals of all of the switching flip-flops from the restorer pulse generator. These pulses are approximately 0.25 microsecond wide and 25 volts in amplitude. The second pulse is smaller than the first because of attenuation in the delay line on the input of the restorer pulse generator.

Figs. F-143-2 and F-143-3 show the set and reset pulses respectively. The reason for the poor shape of these pulses is that they are driving the flip-flops direct from the differentiating network without intermediate amplification; however, they give satisfactory operation.

Fig. F-143-4 shows the waveform on the left grid of the driver V105. This waveform is the same as that of the plate of the "zero" side of the first flip-flop. The figure shows that the left section of V105 is cut "off" following the set pulse and is turned "on" again by the reset pulse. Also, that section of the driver is

turned "off" during the restoring period.

Fig. F-143-5 shows the waveform at the grid of the left section of V104, the 7F8 that aids the driver V105. This waveform is obtained from the right grid of V105, whose voltage is the inverse of the waveform shown in Fig. F-143-4. The sloping top of the pulse is due to distributed capacitance of the matrix being charged through the cathode followers and the charging slope is coupled to the grid through the grid-to-cathode condenser.

Fig. F-143-9 shows the plate of the left section of V105 which is also the left cathode of V104. Initially, the pulse rises up to a peak, but it is pulled down by stray coupling to plate lines that are dropping. Without the 7F8 circuit this drop would continue to slightly below the base line before rising again. With the left section of V105 cutoff, the current drawn by the left section of V104 must pass through the diodes in the back direction, increasing the cathode to ground resistance of the 7F8. The sloping top oc the pulses in Fig. F-143-9 is due to the distributed capacitance of the matrix being charged through the cathode followers.

Fig. F-143-8 is the waveform at the plate of the right section of V105. This waveform is opposite in polarity to that of Fig. F-143-9 and the slope of matrix charging curve is clearly shown.

Fig. F-143-6 shows the waveform at output terminal No. 32 when it is the selected terminal. The rise time of the terminal is longer than that of any of the other terminals since the maximum amount of change has to take place in order to switch from terminal No. 1 to 32. In Fig. F-143-6, the heavy horizontal grid line represents zero voltage and the picture shows that the waveform is clipped above zero. This waveform is a clipped version of Fig. F-143-9.

During the restoring period the switch is switched from line No. 1 to Line No. 32; thus, line No. 32 becomes a selected line for the duration of the restoring period. A positive pulse should appear on line 32, and a negative pulse on line 1 during the restoring period, but no change should occur on any of the other lines. When the flip-flops are triggered on the cathode as with the restorer pulses, both tubes are turned "off" for the duration of the trigger before they "flip". This means that the "off" driver tube is now turned "on" before the "on" tube is turned "off". Consequently, the 7F8 cathode followers are pulsed too soon and their effect is not felt on the plate of the drivers because the drivers are still conducting. When the proper driver tubes are cutoff, the selected

line (line No. 32) rises in voltage at the rate determined by the time constant of the circuit unaided by the pulsed 7F8. This effect is shown in Fig. F-143-6, where the right-hand pulse shows the line being selected during the restoring period. By reducing the amplitude of the restorer pulses to the minimum amplitude providing satisfactory operation, the flip-flop switching time is increased and the restoring period pulse on line 32 can be made to have a fast rise and a flat top. On all output lines except No.'s 1 and 32, small positive transient pulses appear at the beginning and end of the restoring period. This is shown in waveforms Figs. F-143-7 and F-143-10.

Fig. F-143-7 shows the waveform at output line No. 31 during the time line No. 32 is selected. This waveform shows the positive peaks that appear on unselected lines due to the fact that the "on" drivers are always turned "off" slightly before the "off" drivers are turned "on" when the flip-flops are triggered on the grids. This delay is caused by rise time of the driver grid signal in the region where the tube is cutoff.

Fig. F-143-10 shows the selection of line No. 4. Only two flip-flops have to be switched to select this line, and therefore the switching time is slightly less than for line No. 32. Figs. F-143-16 and F-143-17 show expanded views of the selection of lines Nos. 32 and 4 respectively.

Fig. F-143-11 shows the output of No. 4 output amplifier, V604, during the time No. 4 line is selected. The selection of an output turns "on" the associated output amplifier thus producing a negative pulse for the duration of the selection.

The construction of the switch requires that line No. 1 normally be selected except during a restoring operation or during the period in which the switch is used to momentarily select another line. This means that the No. 1 output amplifier operates "on" most of the time. In the test setup, all output amplifiers are identical, using screen dropping resistors and screen by-pass condensers, and therefore, the No. 1 amplifier operates with a lower average screen voltage and puts out much smaller amplitude pulses. In the final switch design the No. 1 amplifier will have to be designed to operate continuously and give an output equal in amplitude to the other amplifiers.

Fig. F-143-12 shows the output of the No. 1 output amplifier during the selection of line No. 4. During the selection of No. 4 and during the restoring operation, Line No. 1 becomes

unselected, hence the negative voltage, indicating selection, rises indicating non-selection.

Fig. F-143-13 shows the voltage waveform at the input to toggle-switch storage register No. 4 during the selection of switch output No. 4. This is also the output of the storage input amplifier, Drawing A-30673. Dead storage in this test was simulated by only four, 16-digit registers made up of toggle switches and crystals as is shown in Drawing A-30676. The cause of the ringing appearing in Fig. F-143-13 was later found to be due to a poor ground connection between the storage panel and the synchroscope.

Fig. F-143-14 shows the voltage waveform at the output of one digit column of the storage registers during the selection of Register No. 4 and with all storage switches in the "on" position. An expanded view of this waveform is shown in Fig. F-143-13. This waveform does not have the amplitude of the waveform of Fig. F-143-13 because the portion below ground has been clipped off. Careful design of the storage input amplifiers to make the lower level of the plate voltage zero, and a clamping circuit in the grid to clamp the top of the input waveform at cathode potential of the amplifier will give a larger storage output pulse.

Fig. F-143-15 shows the output of the same digit column as in Fig. F-143-16, but with the toggle switch representing that digit in Register No. 4 turned off, and all other storage switches closed. The small pulse that is present is due to the input pulse to register No. 4 passing through all of the closed digit switches to the digit output columns. Then, passing through the back resistance of the isolating crystals to the input terminals of the other registers, the pulse appears on the digit column being observed.

Further Work to be Done on the Switch

The present model of the 32-position electronic switch has proved that such a switch is feasible and can be made to work with a switching time of less than two tenths of a microsecond. The remainder of the work to be done on the switch consists mainly in modifications and refinements of the present circuits for more efficient operation. The components needing investigation and modification are the 7F8 cathode follower circuits, the output amplifiers, and the storage input amplifiers. These three circuits were not designed for efficient operation, but merely to test the effects of such circuits. The circuits apparently perform their

assigned functions and therefore warrant more detailed study.

The 7F8 circuits have two functions as previously mentioned, to cancel the stray capacitively coupled voltages and to provide a higher voltage to effect the rise of the selected terminal. By removing the 7F8's entirely from the circuit and connecting 47K resistors from +150 volts to the plates of all driver tubes, the rise time of the switching signal is considerably increased, but the drop occurring after the initial rise is enough to bring the voltage back down to the unselected level before rising again. The switching time with such a circuit is 0.5 microsecond as compared to the original one microsecond. This indicates that the 7F8's actually do oppose the unwanted drop. The photographs show that the grid of the 7F8 never goes positive with respect to the cathode; therefore, the 7F8 tubes do not draw more than the zero bias current of about 12 milliamperes. This is a plate dissipation of about 1.8 watts whereas the tube is rated at 1.75 watts per section. In the final design, all tubes should operate at half rating and this will require that a larger tube than the 7F8 be used. However, the zero grid current of such a tube must be about that of the 7F8, or during the period for which the driver is off the voltage may rise high enough to exceed the back voltage of the crystals. With the 7F8 circuit it is estimated from Fig. E-143-8 that the maximum back voltage occurring across the crystals is about 30 volts.

The switch output amplifiers must be designed so as to allow the maximum length of pulse expected to be coupled to storage and, as mentioned previously, the amplifier of line No. 1 must operate at a duty cycle of about ninety per cent. The storage input amplifiers should be changed to insure maximum amount of signal applied to storage, and the grid circuits should be clamped.

Engineer: John P. O'Brien

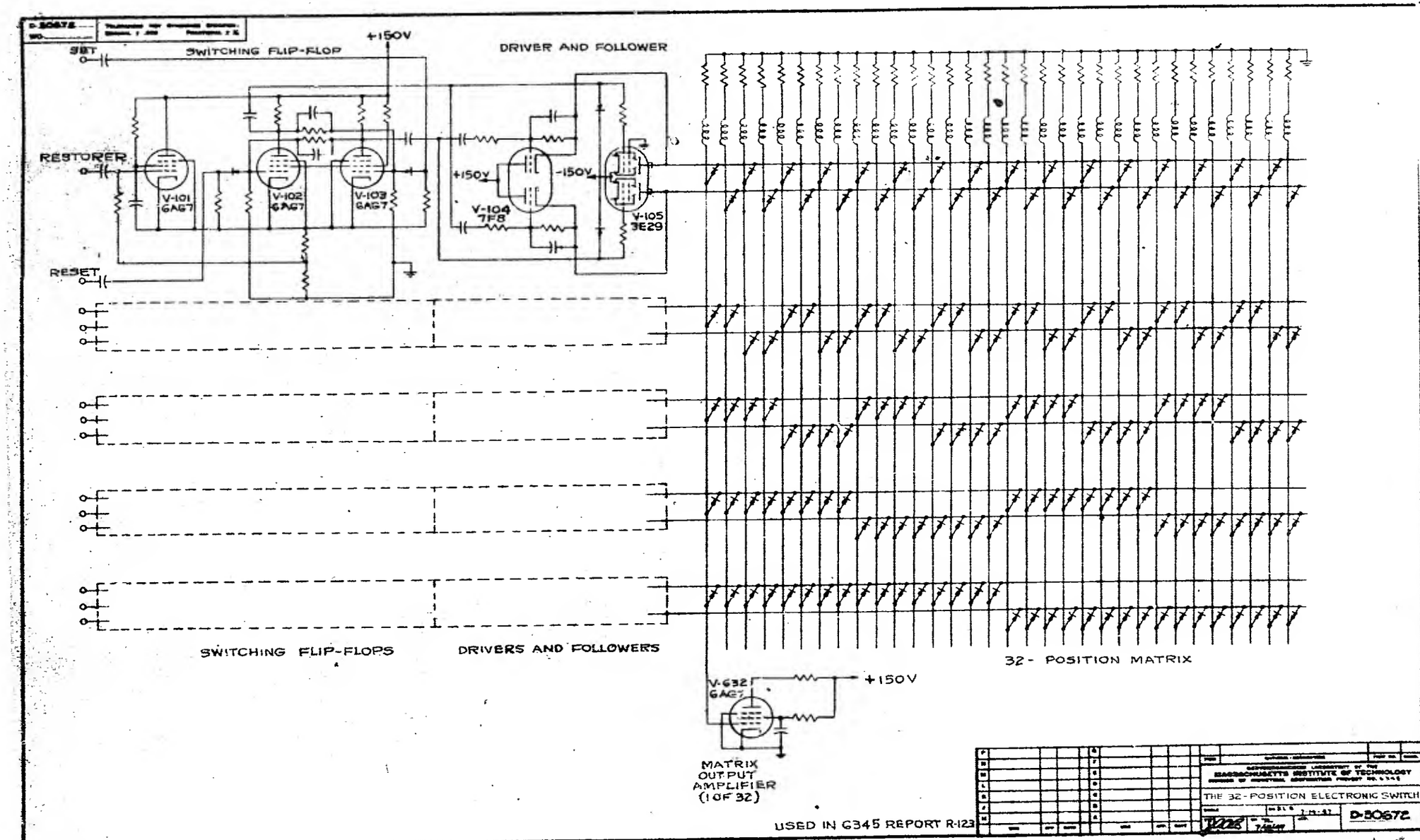
Approved: Jay W. Forrester

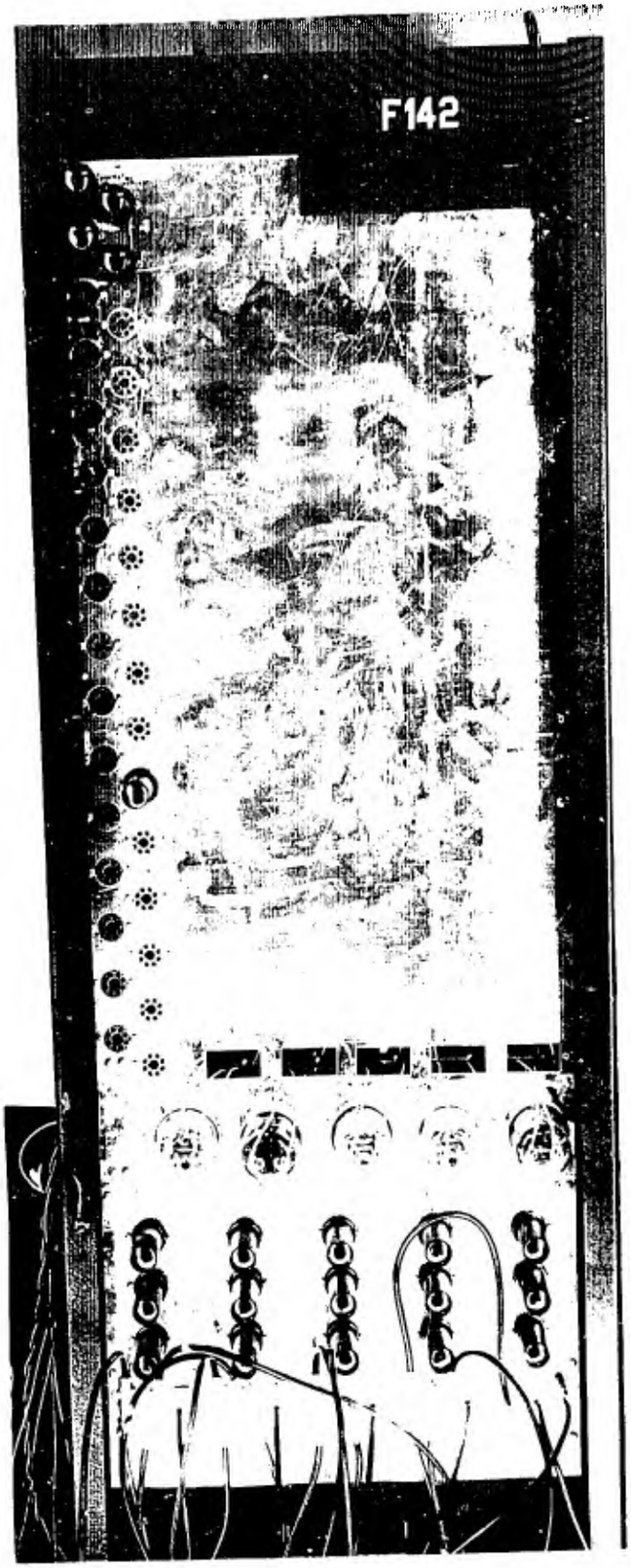
JAO'B:hes

APPENDIX

LIST OF DRAWINGS

Drawing No.	Title
D-30672	The 32-Position Electronic Switch
A-30696	Rear View of the 32-Position Switch Rack
A-30695	Laboratory Setup for Testing the 32-Position Switch
A-30694	Crystal Matrix and Toggle Switch Storage Used in the 32-Position Switch
A-30676	32-Position Matrix
A-30693	Flip-Flops and Drivers of the 32-Position Switch
A-30678	Crystal Matrix Static Test Setup
A-31237-2	Switching Flip-Flops
A-31667	Drivers and Followers for 32-Position Switch
B-30677-1	Test Setup for 32-Position Switch
A-30457	Pulse Sharpener
A-31847-3	Restorer Pulse Generator
A-30674	Differentiator and Clipper, and Toggle-Switch Coder
A-30673	32-Position Switch Output Amplifiers
A-30675	Toggle-Switch Storage
A-30668) A-30669) A-30670) A-30671)	Figures F-143-1 to F-143-18 inclusive. Waveform of the 32-Position Switch


SET
SWITCHING FLIP-FLOP
+150V
DRIVER AND FOLLOWER
RESTORER
V-101 6AG7
V-102 6AG7
V-103 6AG7
+150V
-150V
V-104 7F8
V-105 3E29
RESET
SWITCHING FLIP-FLOPS
DRIVERS AND FOLLOWERS
32 - POSITION MATRIX
V-632 6AG7
+150V
MATRIX OUTPUT AMPLIFIER (1 OF 32)
USED IN G345 REPORT R-123
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
THE 32 - POSITION ELECTRONIC SWITCH
D-50672



MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

D. I. C. NO. 6345	DR.	CK.
ENG. J. A. O'B	APP.	A-30696

A-30696

REAR VIEW OF THE 32-POSITION SWITCH RACK

USED IN 6345 REPORT R-123

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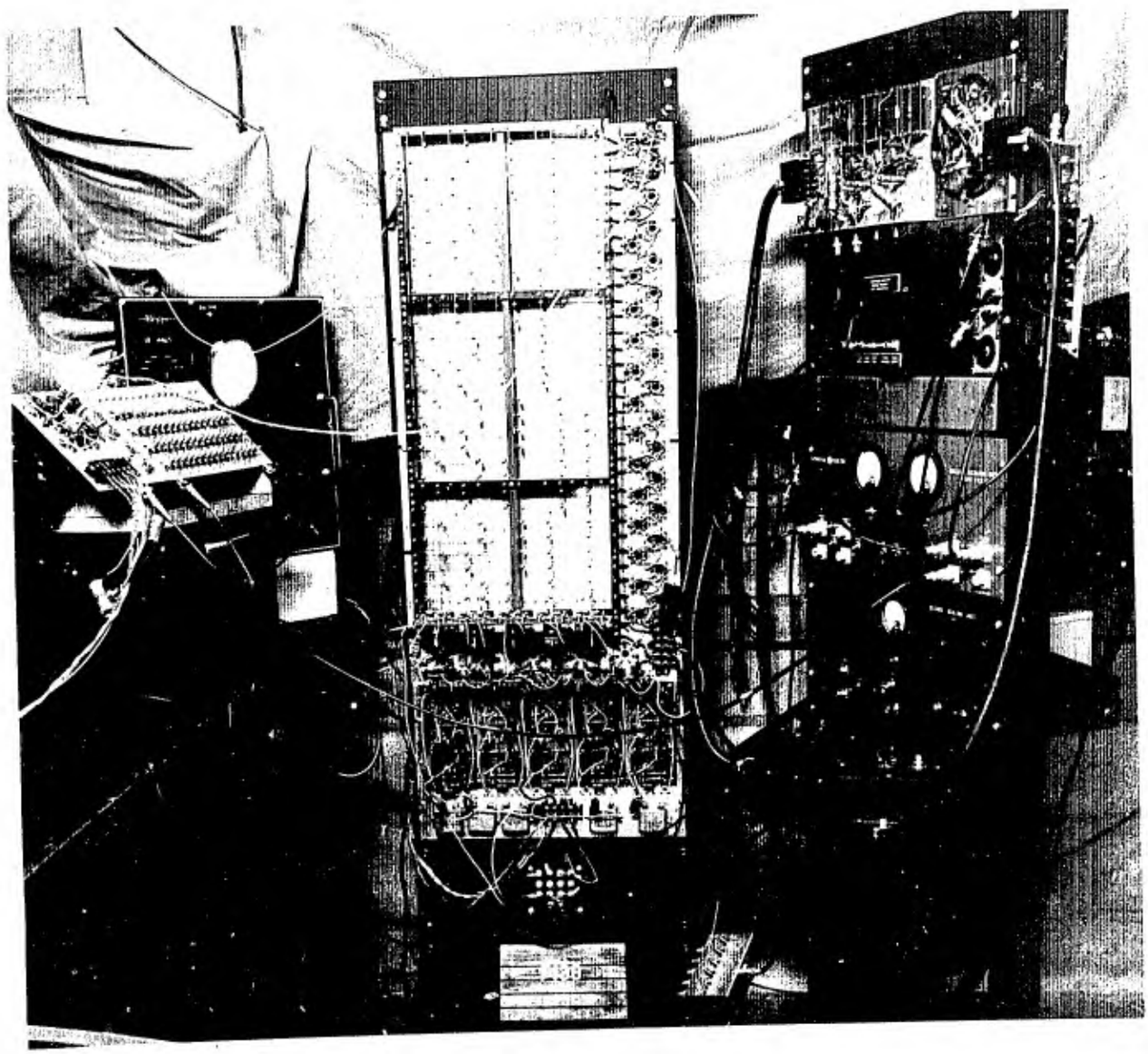
ENG. J.A.O'B	APP.	A-30695

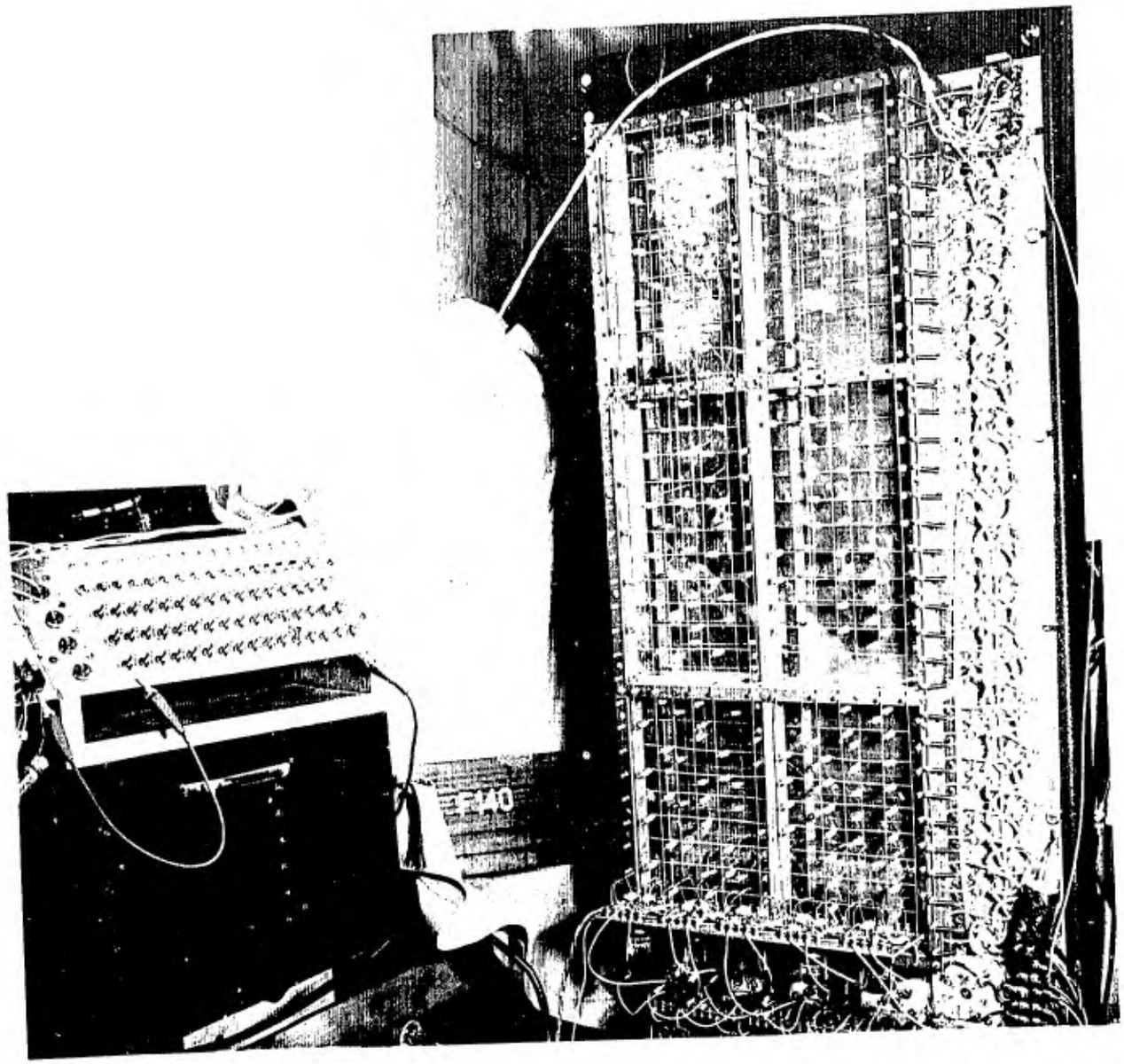


LABORATORY SET UP FOR TESTING
THE 32 POSITION SWITCH

A-30695

USED IN 6345 REPORT R-123

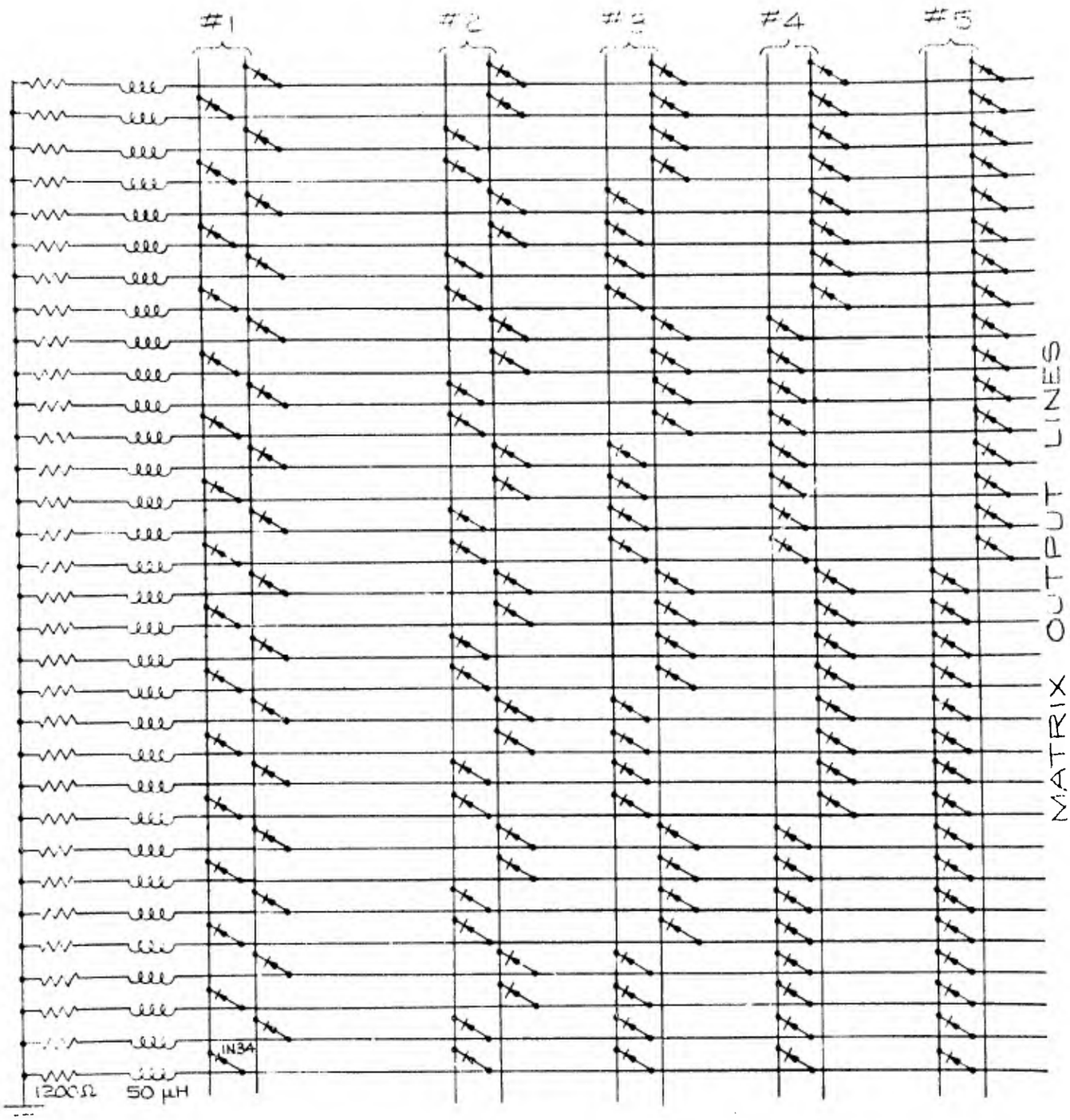
MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. I. C. NO. 6345	DR.	CK.
ENG. J.A.O'B	APP.	A-30694



CRYSTAL MATRIX AND TOGGLE SWITCH STORAGE
USED IN THE 32 POSITION SWITCH

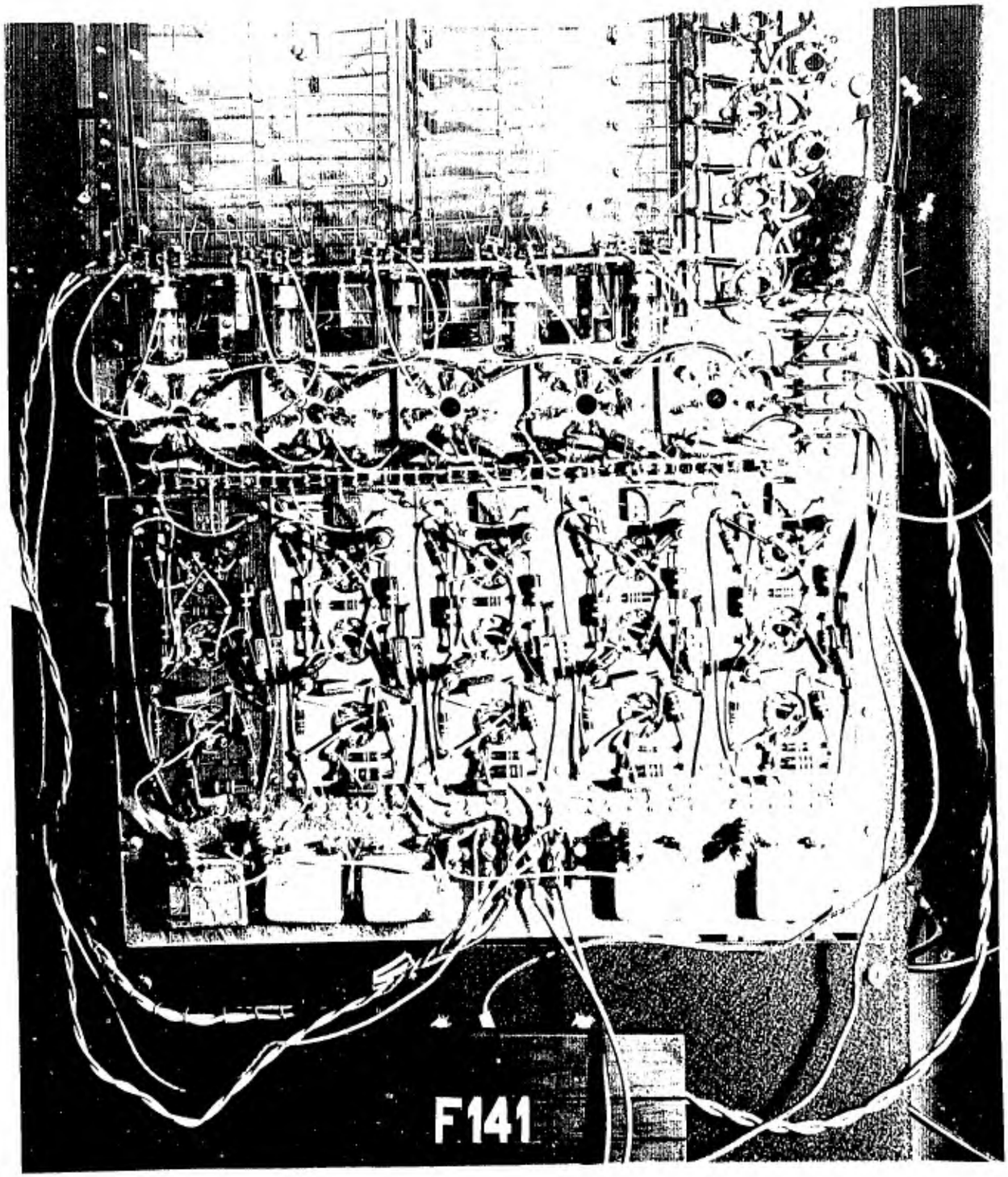
A-30694

USED IN 6345 REPORT R-123



32-POSITION MATRIX

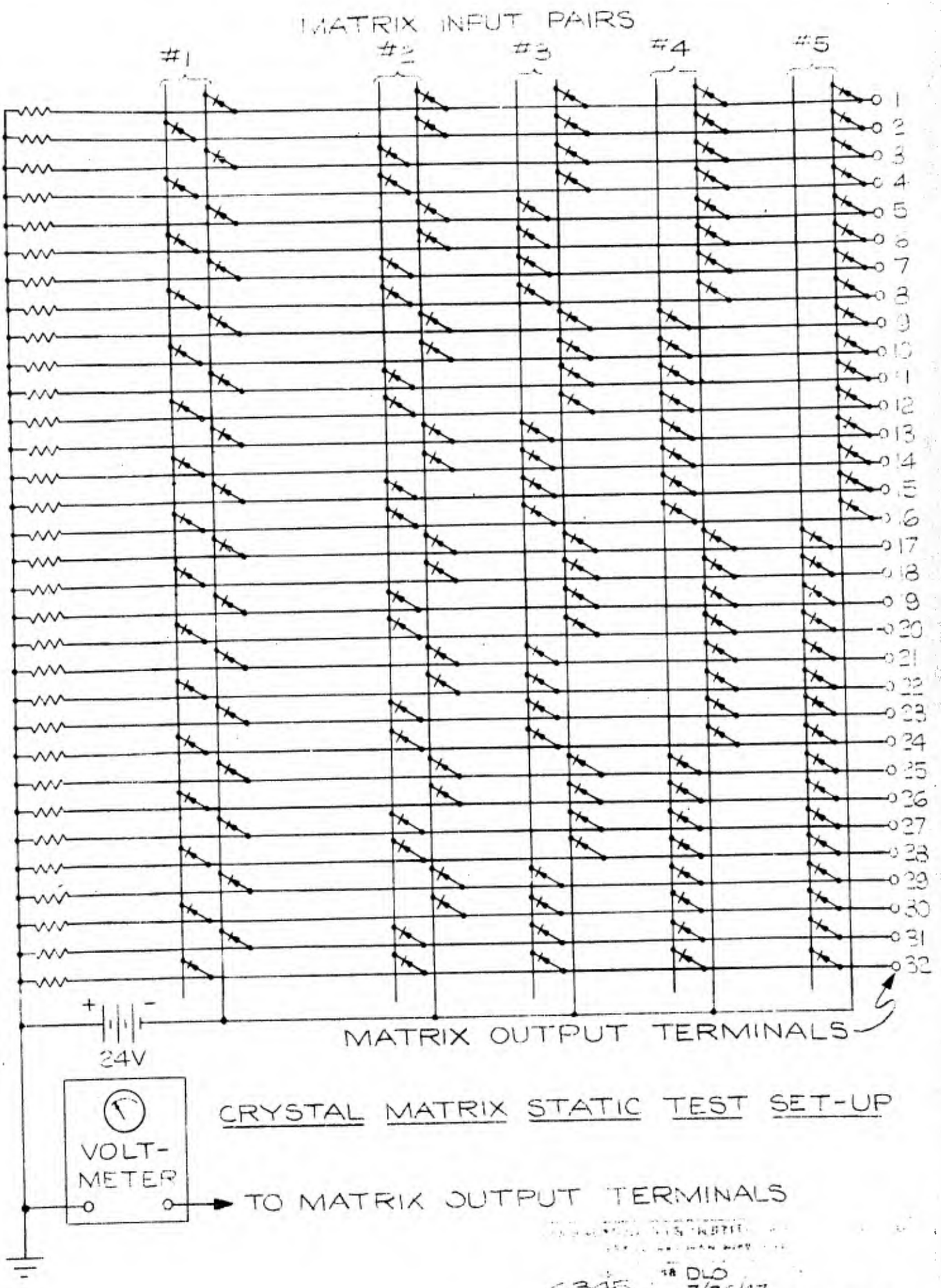
MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. I. C. NO. 6345	DR.	CK.
ENG. J.A.O'B	APP.	A-30693



FLIP-FLOPS AND DRIVERS OF THE
32 POSITION SWITCH

A-3069-

USED IN 6345 REPORT R-123



CRYSTAL MATRIX STATIC TEST SET-UP

DLO
7/24/47

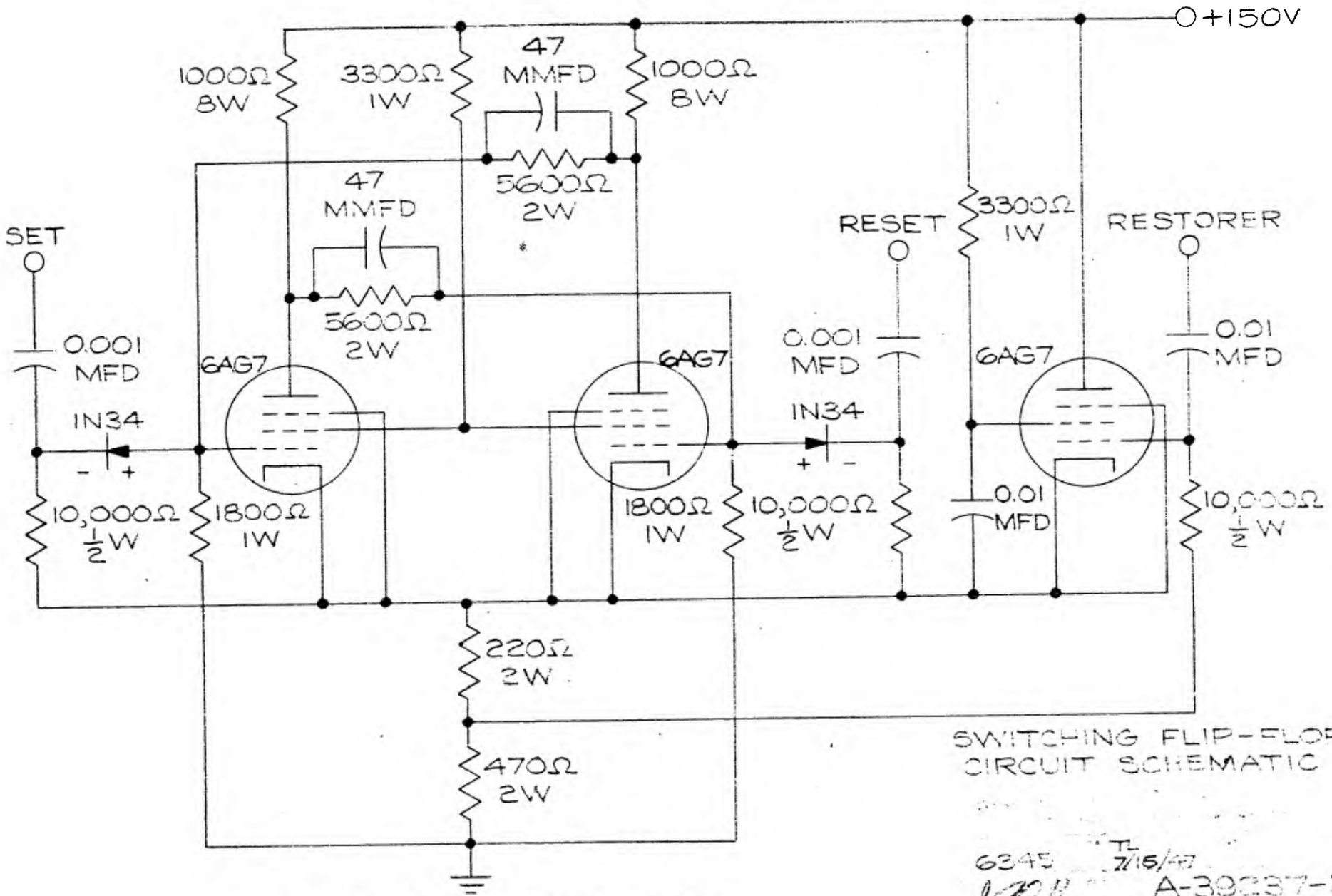
6345
1400

A-30673

USED IN 6345 REPORT R-123

A-30678

A-39237-?

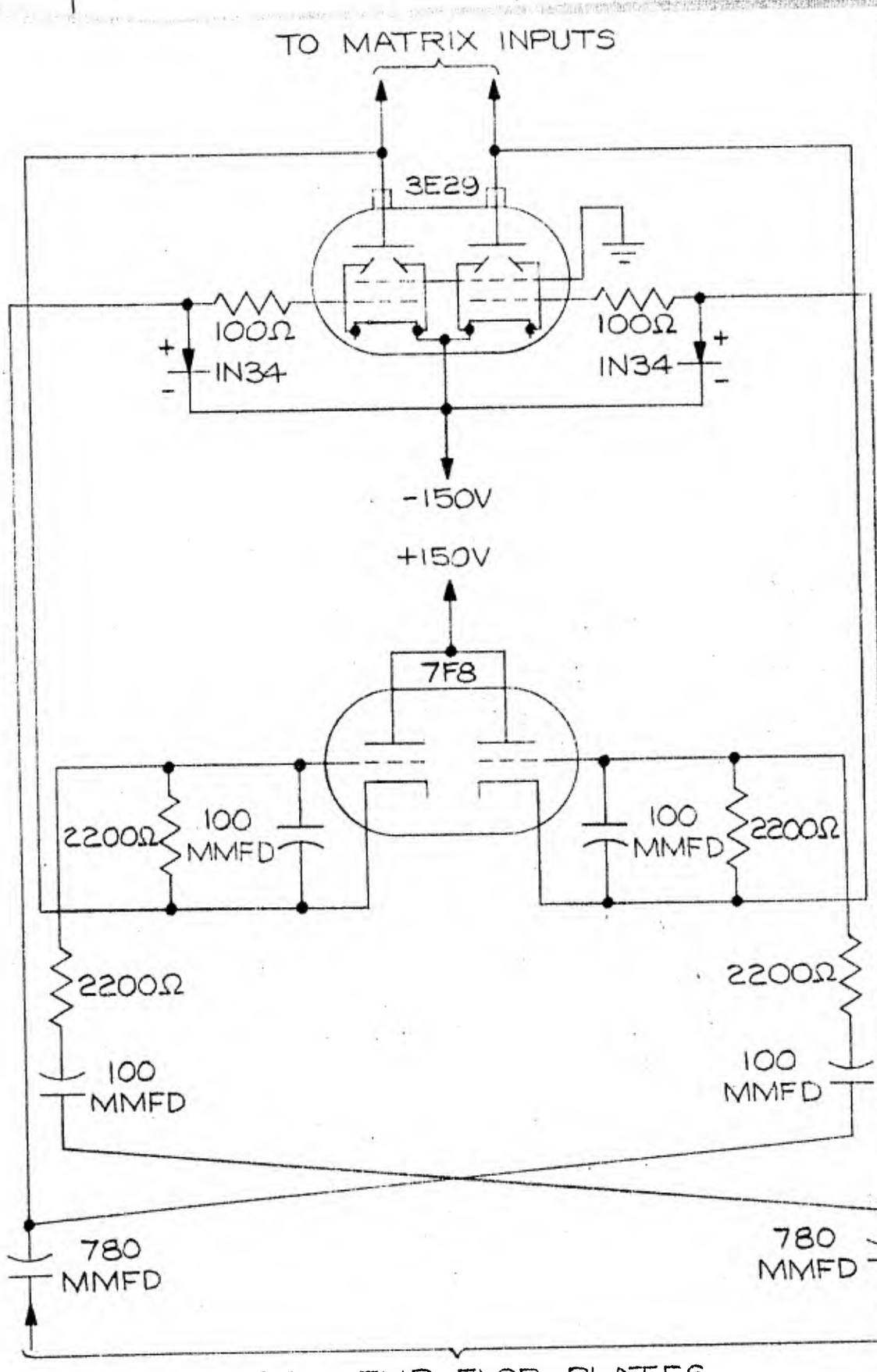


SWITCHING FLIP-FLOP CIRCUIT SCHEMATIC

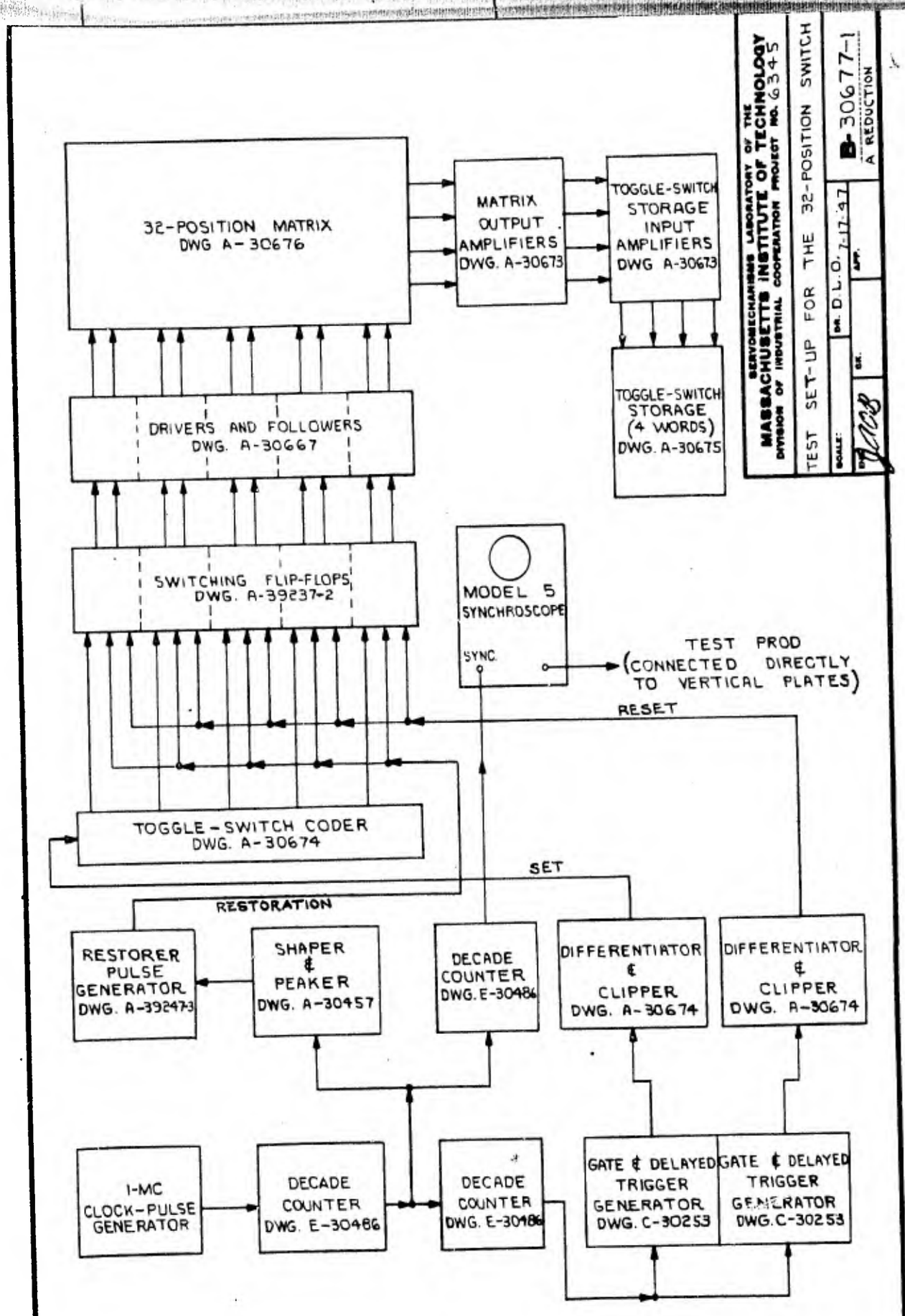
USED IN 6345 REPORT R-123

6345 TL 7/16/47

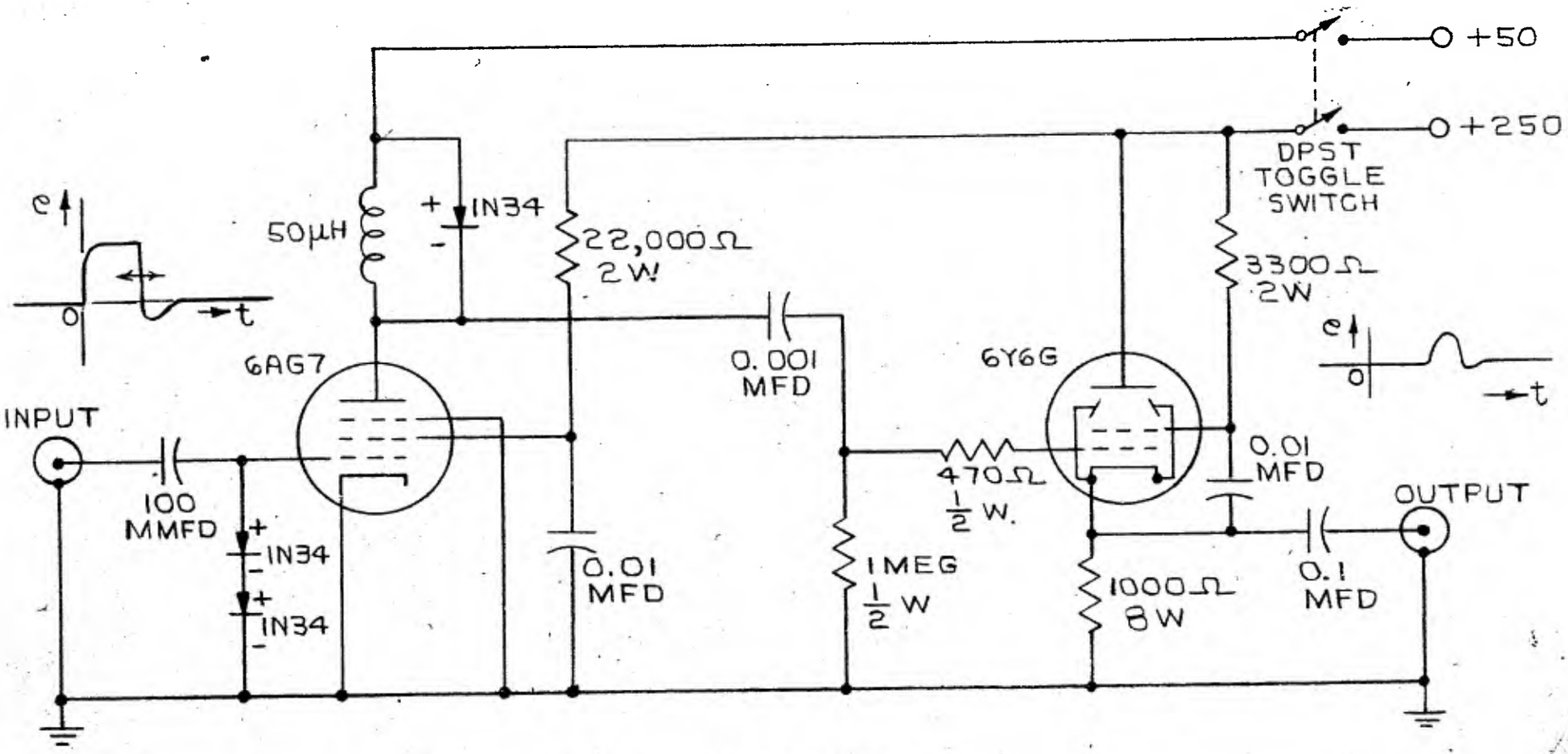
A-39237-2



DRIVERS AND FOLLOWERS
FOR 32-POSITION SWITCH


32-POSITION MATRIX
DWG A-30676
MATRIX OUTPUT AMPLIFIERS
DWG. A-30673
TOGGLE-SWITCH STORAGE INPUT AMPLIFIERS
DWG A-30673
TOGGLE-SWITCH STORAGE (4 WORDS)
DWG. A-30675
DRIVERS AND FOLLOWERS
DWG. A-30667
SWITCHING FLIP-FLOPS
DWG. A-39237-2
MODEL 5 SYNCHROSCOPE
SYNC.
TEST PROD
(CONNECTED DIRECTLY TO VERTICAL PLATES)
RESET
TOGGLE-SWITCH CODER
DWG. A-30674
SET
RESTORATION
RESTORER PULSE GENERATOR
DWG. A-392473
SHAPER & PEAKER
DWG. A-30457
DECADE COUNTER
DWG. E-30486
DIFFERENTIATOR & CLIPPER
DWG. A-30674
DIFFERENTIATOR & CLIPPER
DWG. A-30674
1-MC CLOCK-PULSE GENERATOR
DECADE COUNTER
DWG. E-30486
DECADE COUNTER
DWG. E-30486
GATE & DELAYED TRIGGER GENERATOR
DWG. C-30253
GATE & DELAYED TRIGGER GENERATOR
DWG. C-30253
SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345
TEST SET-UP FOR THE 32-POSITION SWITCH
B-30677-1
A REDUCTION
DR. D.L.O. 7-17-47
SCALE:
CK.
APP.
B-30677-1
USED IN 6345 REPORT R-123

A-30457

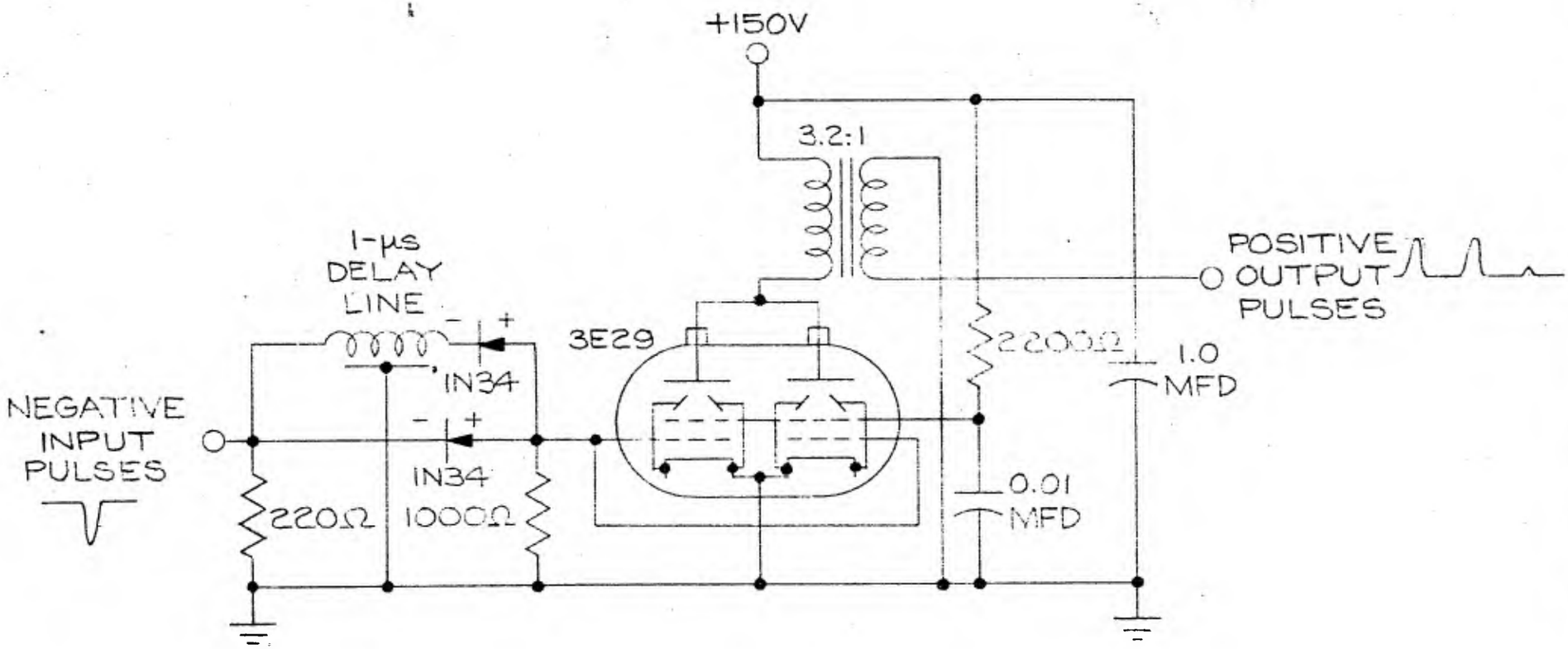


PULSE SHARPENER

USED IN 6345 REPORTS R-120 & R-123

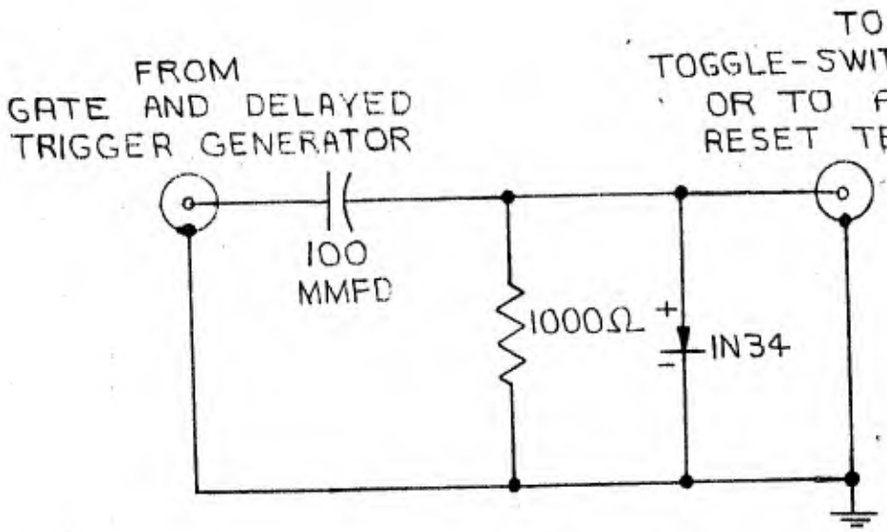
6345	DLO 4/12/47	TH 4/12/47
DL.		A-30457

A-39247-3

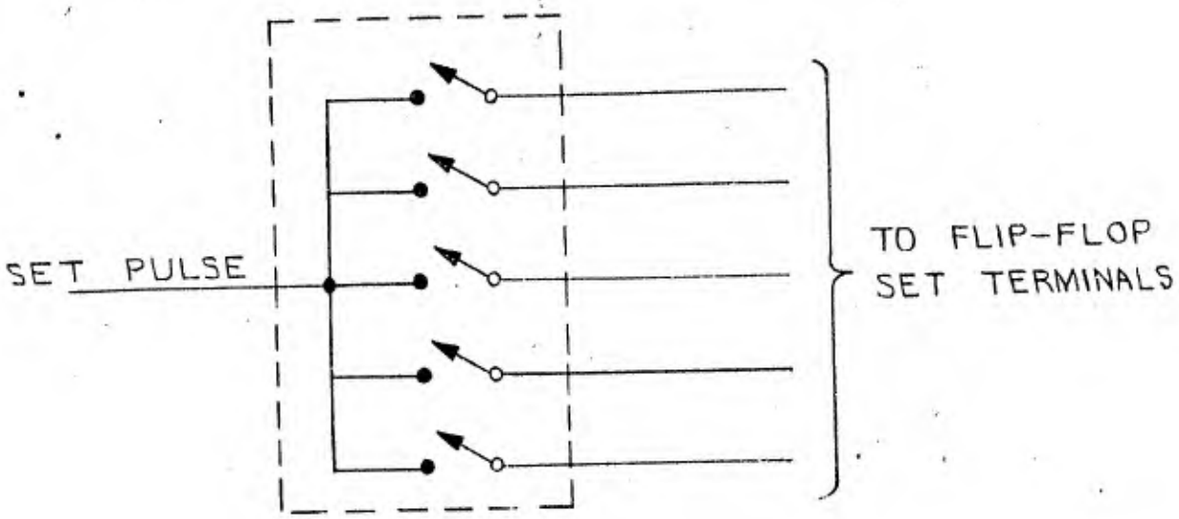


RESTORER PULSE GENERATOR

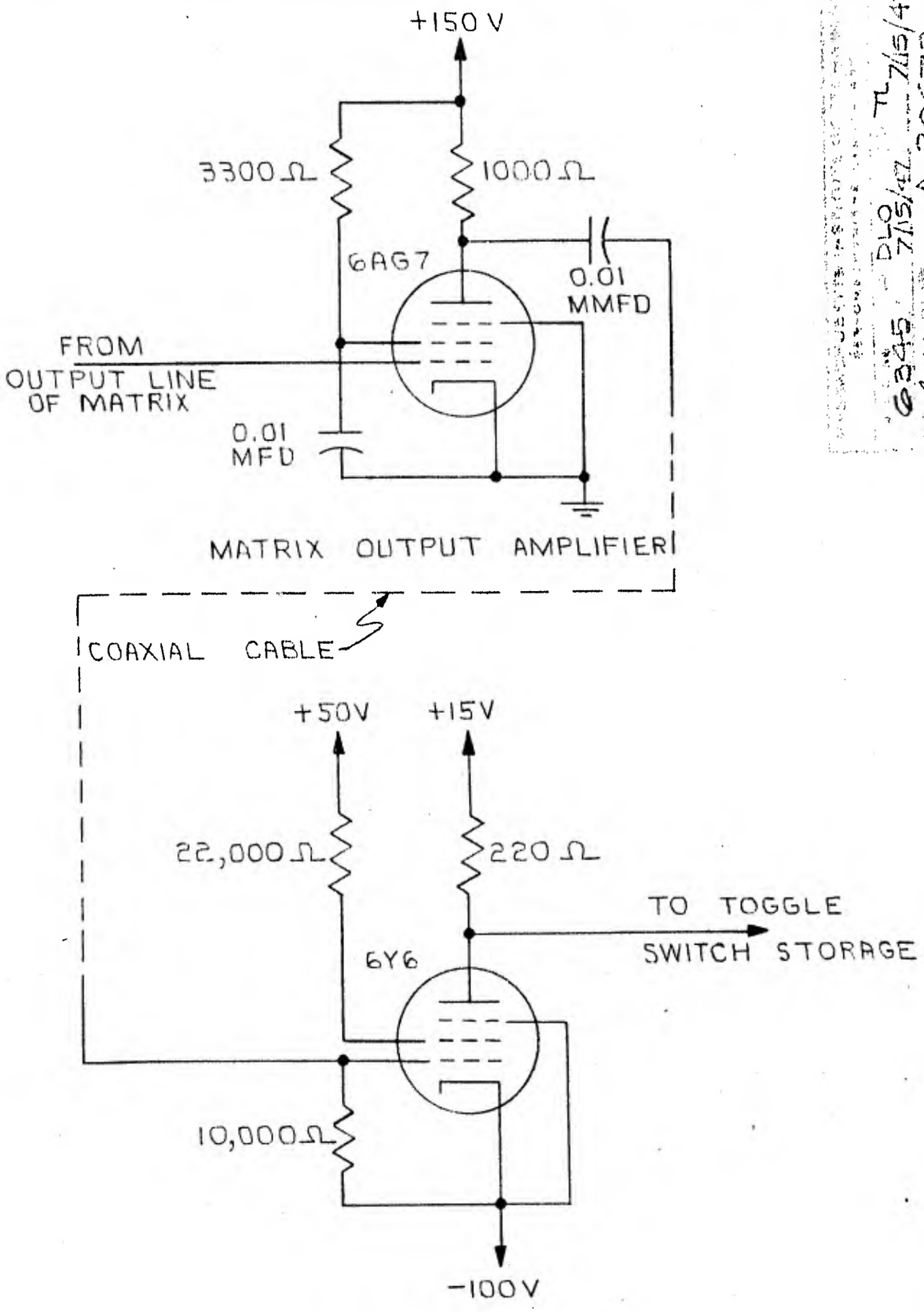
USED IN 6345 REPORT R-123



DIFFERENTIATOR AND CLIPPER



TOGGLE SWITCH CODER

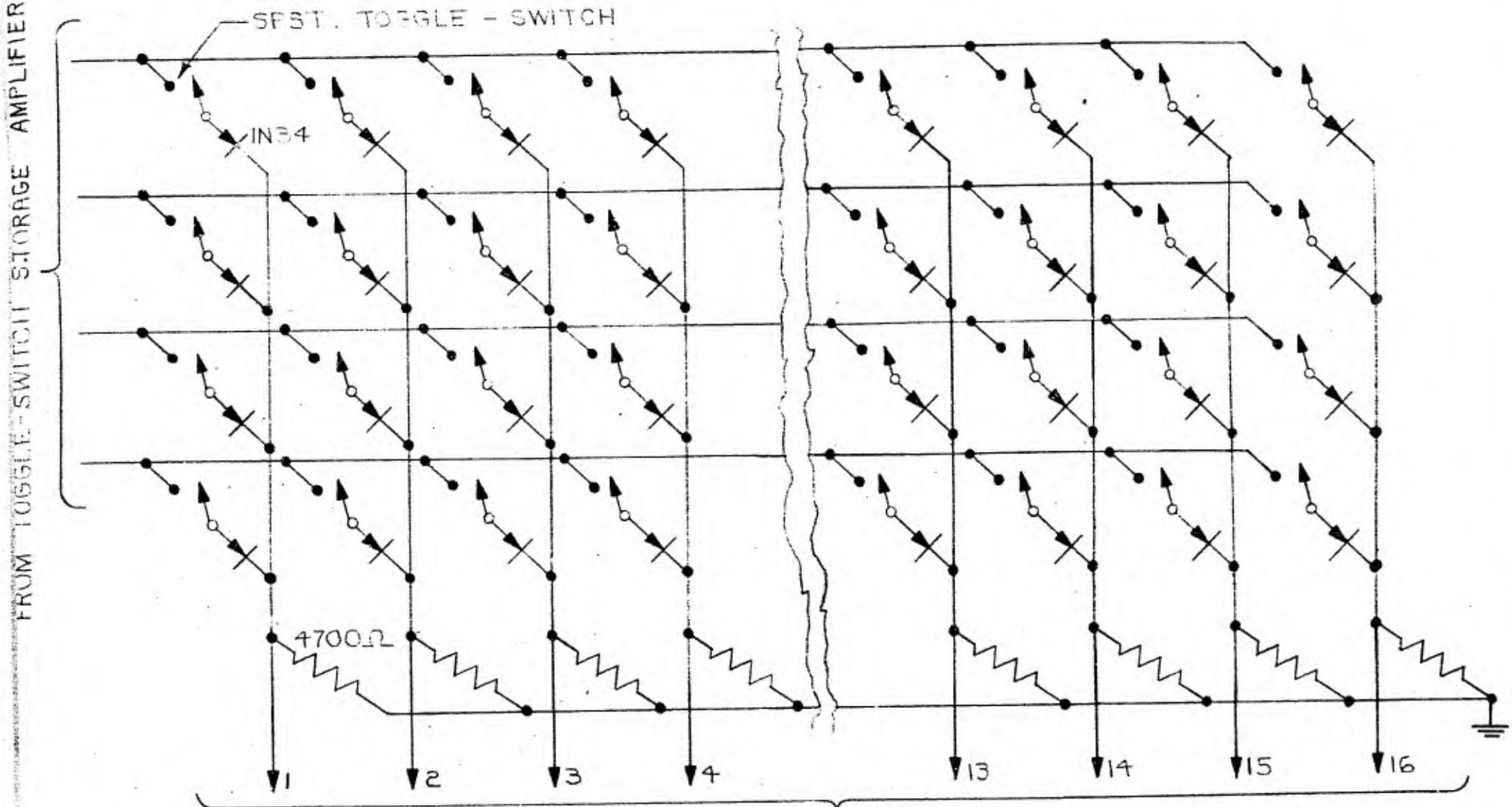


TOGGLE-SWITCH STORAGE INPUT AMPLIFIER

32-POSITION SWITCH OUTPUT AMPLIFIERS

USED IN 6345 REPORT R-123

A-30675



TOGGLE-SWITCH STORAGE (FOUR WORDS)

USED IN 6345 REPORT R-127

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

DIC NO	Dr. D.L.O.
6345	7-16-47
ENG 1408	A-30675

F-143-1

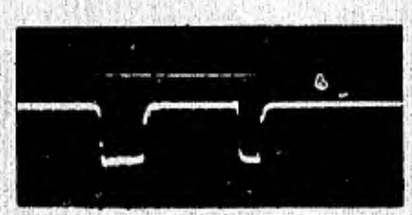
RESTORER PULSES

F-143-2

SET PULSE

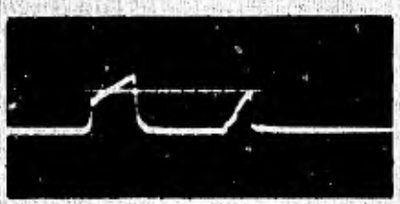
F-143-3

RESET PULSE



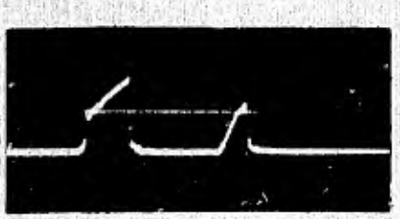
F-143-4

LEFT GRID OF V-105 (3E29)



F-143-5

LEFT GRID OF V-104 (7F8)



F-143-9

LEFT PLATE OF V-105

32- POSITION SWITCH WAVEFORMS

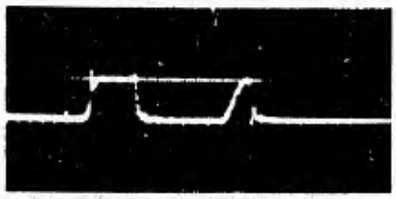
HORIZONTAL SCALE 0.5 MICROSECONDS / SMALL DIVISION

VERTICAL SCALE 6.2 VOLTS / SMALL DIVISION

USED IN REPORT R-123

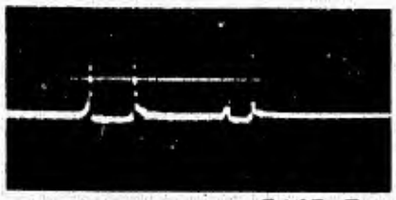
F-143-8

RIGHT PLATE OF V-105



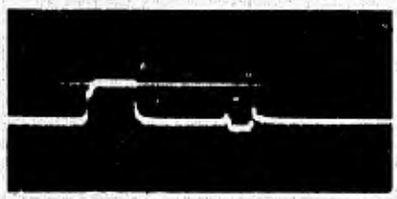
F-143-6

LINE #32 DURING SELECTION



F-143-7

LINE #31 DURING SELECTION OF LINE #32

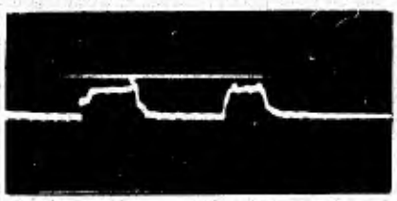


F-143-10

LINE #4 DURING SELECTION

F-143-11

PLATE OF #4 OUTPUT AMPLIFIER V-604
DURING SELECTION



F-143-12

PLATE OF #1 OUTPUT AMPLIFIER V-601
DURING SELECTION OF LINE #4

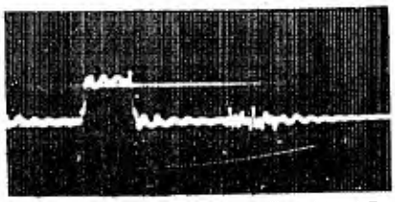
32-POSITION SWITCH WAVEFORMS

HORIZONTAL SCALE 0.5 MICROSECONDS / SMALL DIVISION

VERTICAL SCALE 6.2 VOLTS / SMALL DIVISION

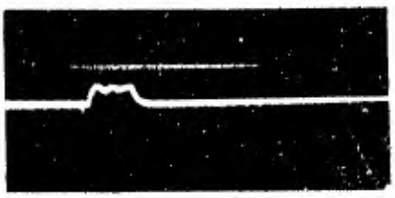
A-30660

USED IN REPORT R-123



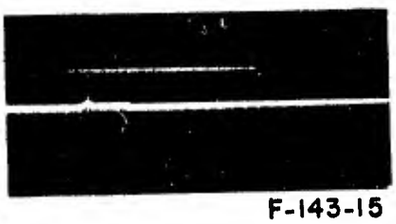
F-143-13

INPUT TO STORAGE REGISTER #4
DURING SELECTION



F-143-14

OUTPUT OF AN "ON" DIGIT OF STORAGE
REGISTER #4 DURING SELECTION
ALL STORAGE DIGIT SWITCHES ON



F-143-15

OUTPUT OF AN "OFF" DIGIT OF STORAGE
REGISTER #4 DURING SELECTION
ALL OTHER STORAGE DIGIT SWITCHES ON

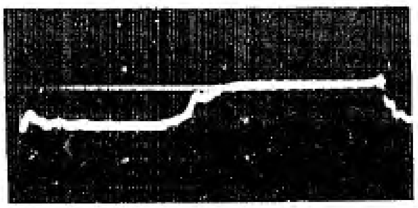
32-POSITION SWITCH WAVEFORMS

HORIZONTAL SCALE 0.5 MICROSECONDS/SMALL DIVISION

VERTICAL SCALE 6.2 VOLTS/SMALL DIVISION

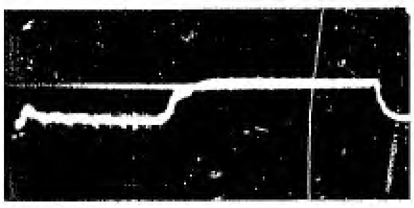
A-30670

USED IN REPORT R-123



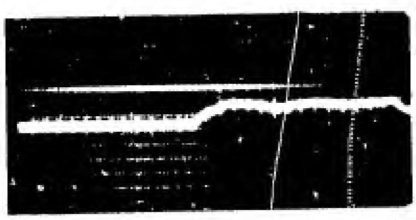
F-143-16

LINE #32 DURING SELECTION
SAME WAVE FORM AS F-143-6



F-143-17

LINE #4 DURING SELECTION
SAME WAVE FORM AS F-143-10



F-143-18

OUTPUT OF AN "ON" DIGIT OF STORAGE
REGISTER #4 DURING SELECTION
SAME WAVE FORM AS F-143-14

32-POSITION SWITCH WAVEFORMS

HORIZONTAL SCALE OF 0.1 MICROSECONDS/SMALL DIVISION
VERTICAL SCALE OF 6.2 VOLTS PER SMALL DIVISION

USED IN REPORT R-123